



Fig. 1
Prior Art

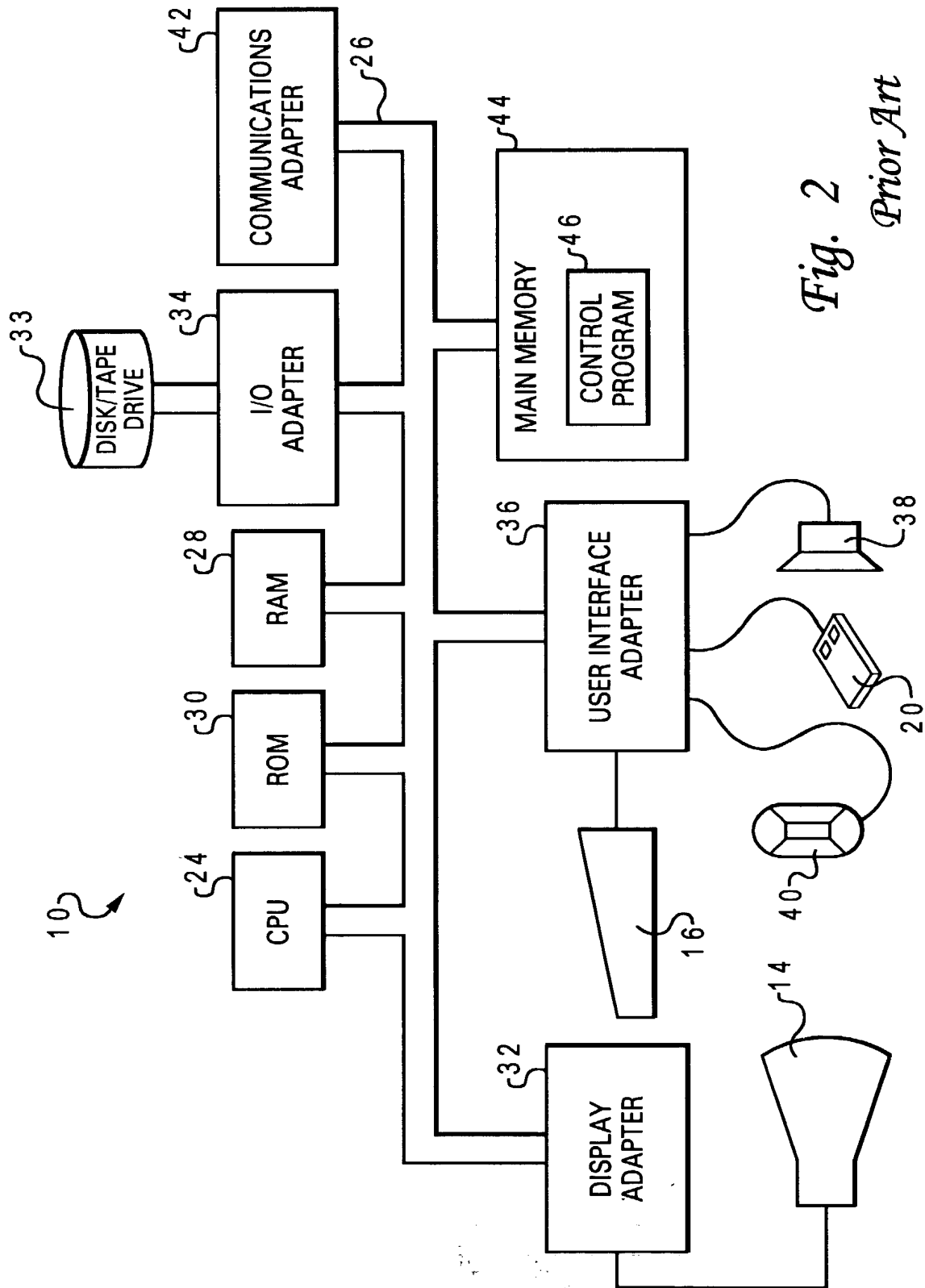


Fig. 2
Prior Art

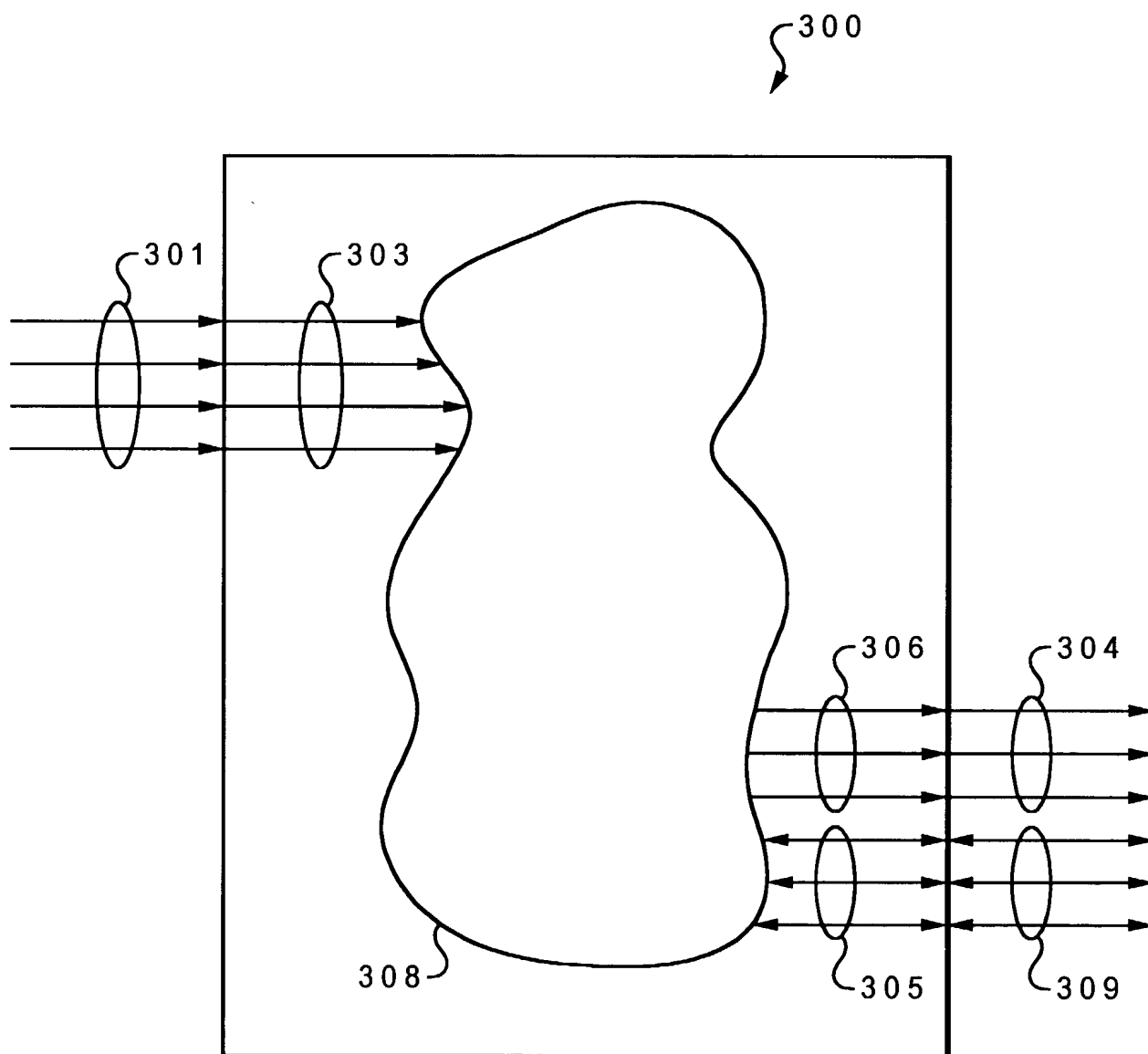
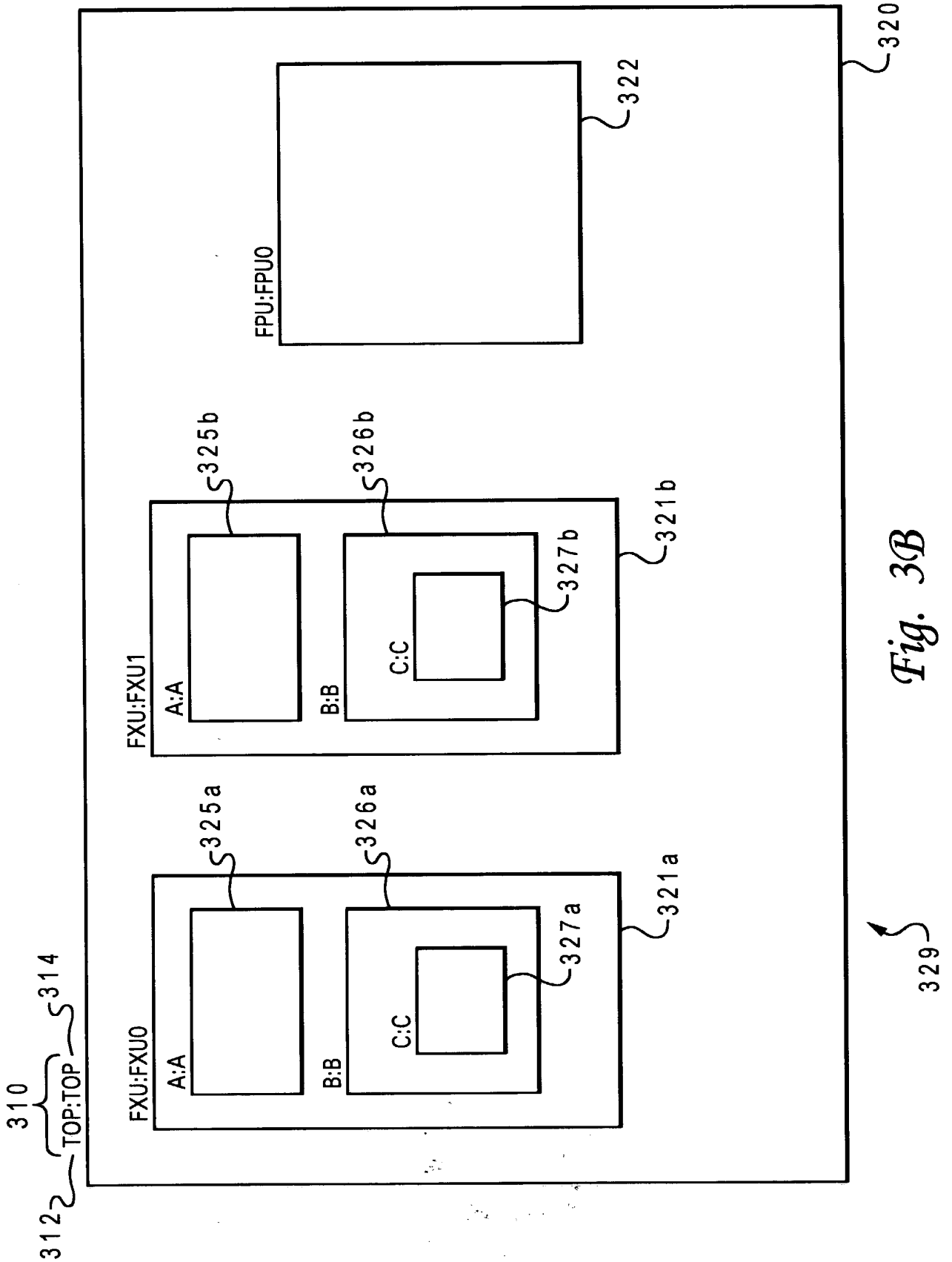
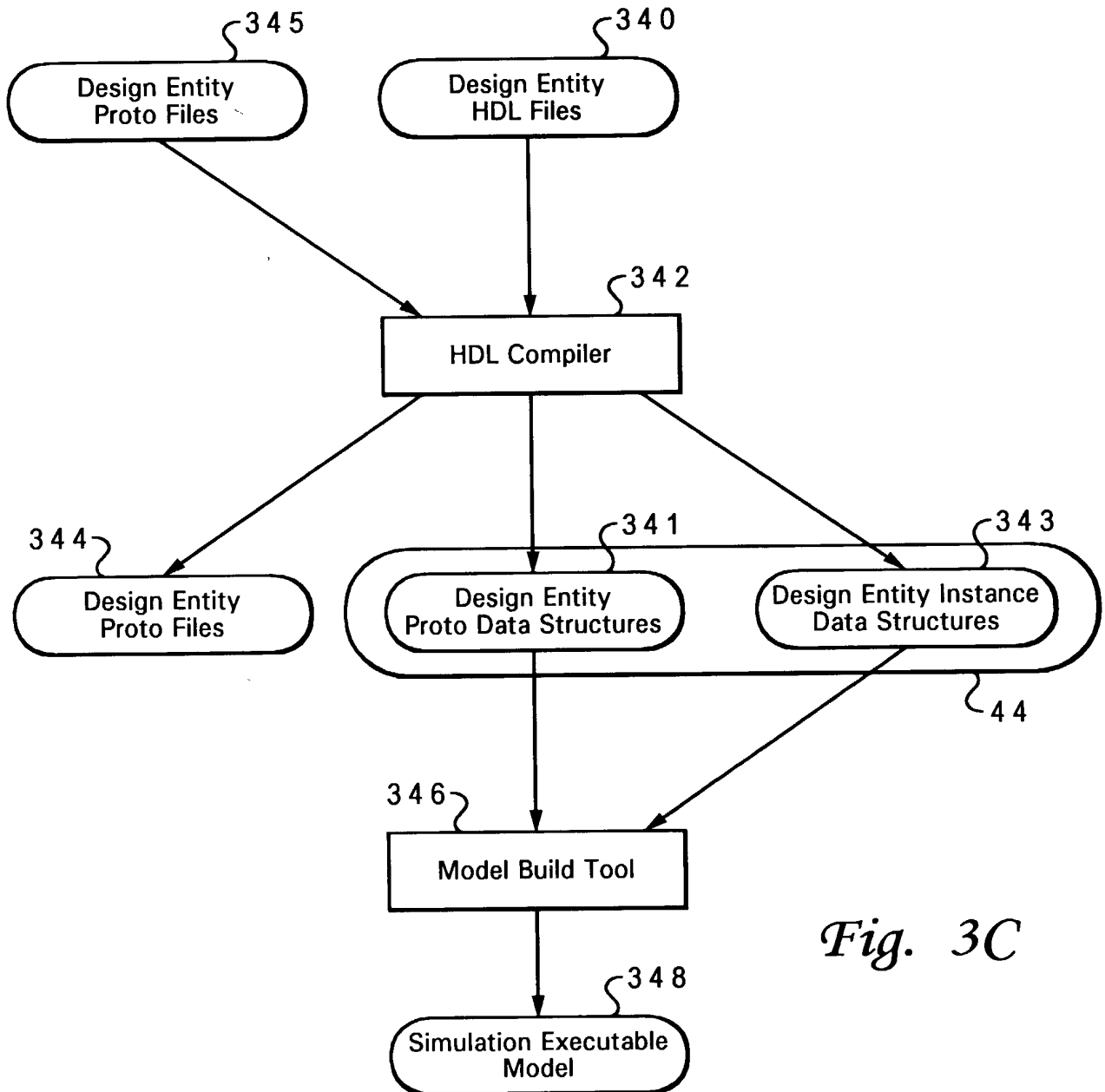


Fig. 3A



*Fig. 3C*

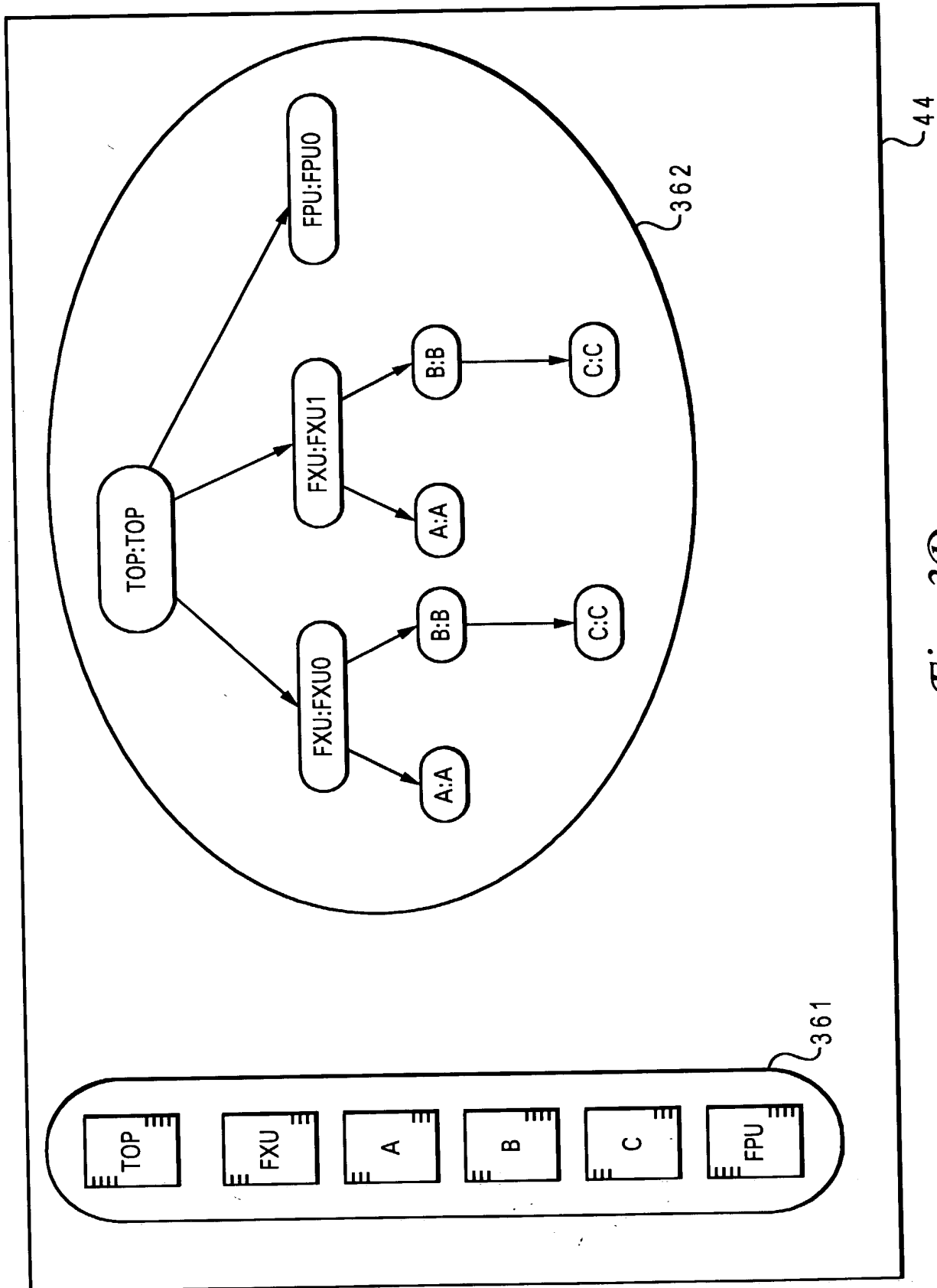


Fig. 3D

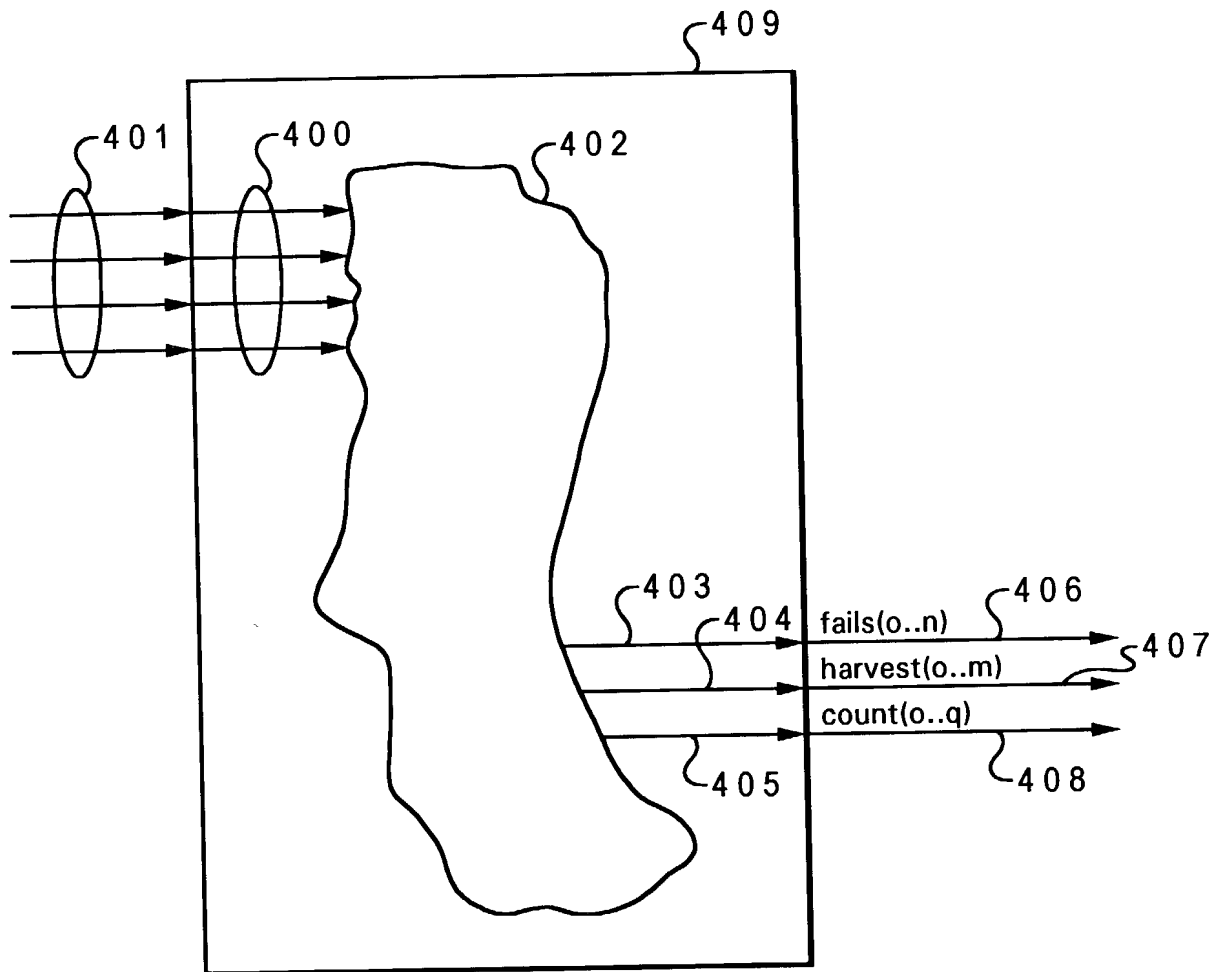


Fig. 4A

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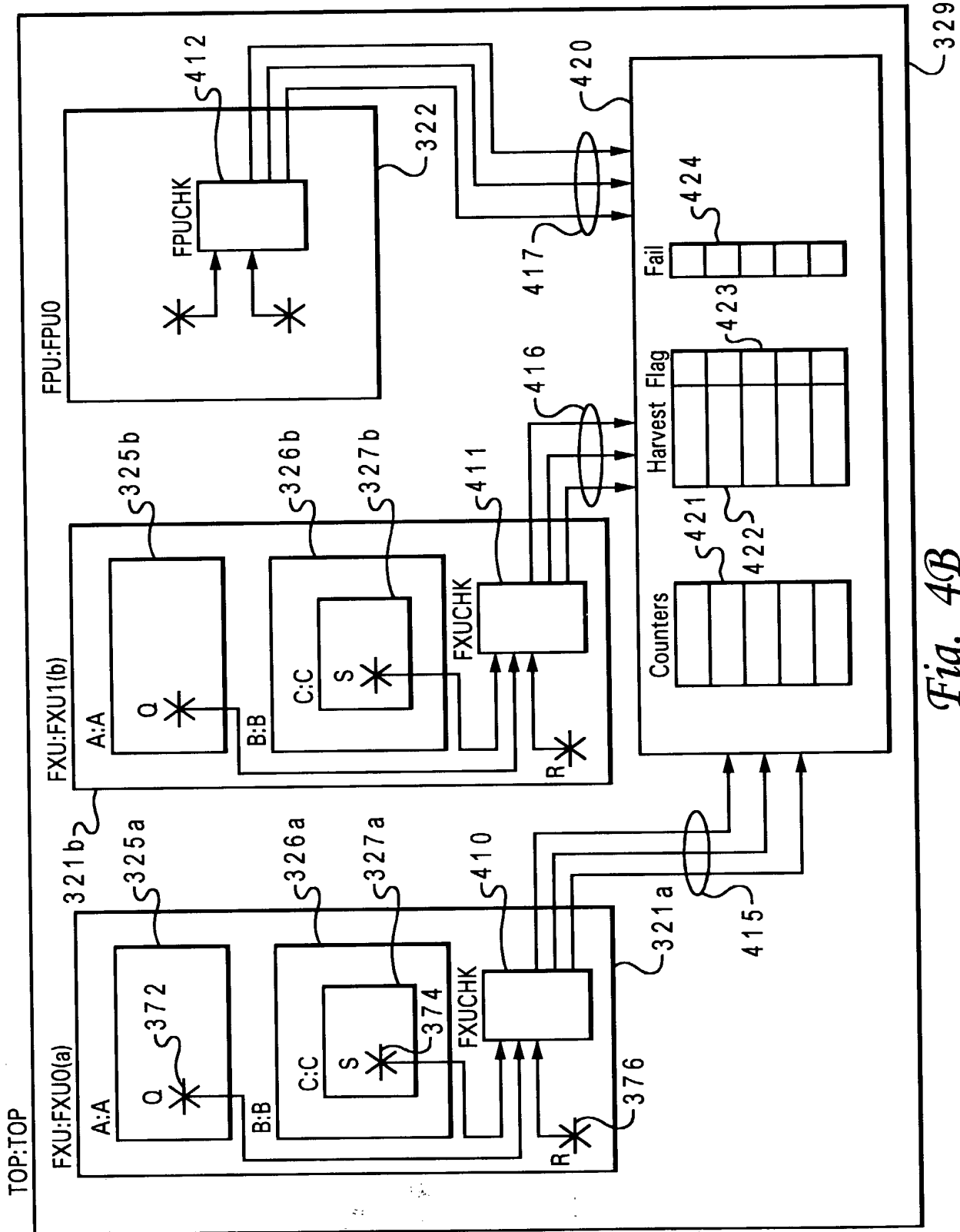


Fig. 4B

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ENTITY FXUCHK IS

```

PORT(  S_IN      :  IN std_ulogic;
        Q_IN      :  IN std_ulogic;
        R_IN      :  IN std_ulogic;
        clock     :  IN std_ulogic;
        fails     :  OUT std_ulogic_vector(0 to 1);
        counts    :  OUT std_ulogic_vector(0 to 2);
        harvests  :  OUT std_ulogic_vector(0 to 1);
);
    
```

4 5 0

4 5 2 { --!! BEGIN
--!! Design Entity: FXU;

4 5 3 { --!! Inputs
--!! S_IN ==> B.C.S;
--!! Q_IN ==> A.Q;
--!! R_IN ==> R;
--!! C_CLOCK ==> clock;
--!! End Inputs

4 5 4 { --!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

4 5 1

4 5 5 { --!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

4 5 7 { --!! End;

4 4 0

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

4 5 8

Fig. 4C

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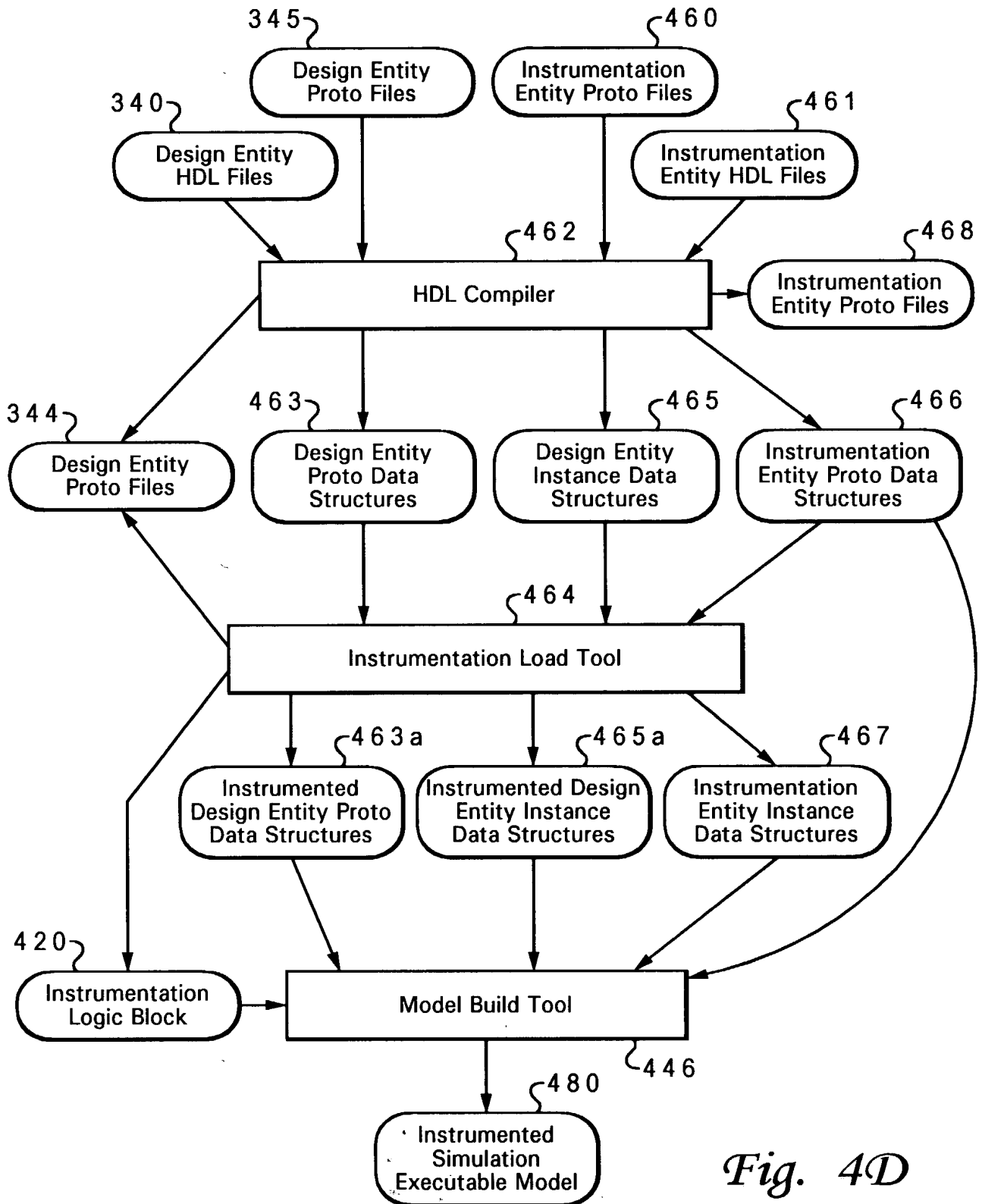


Fig. 4D

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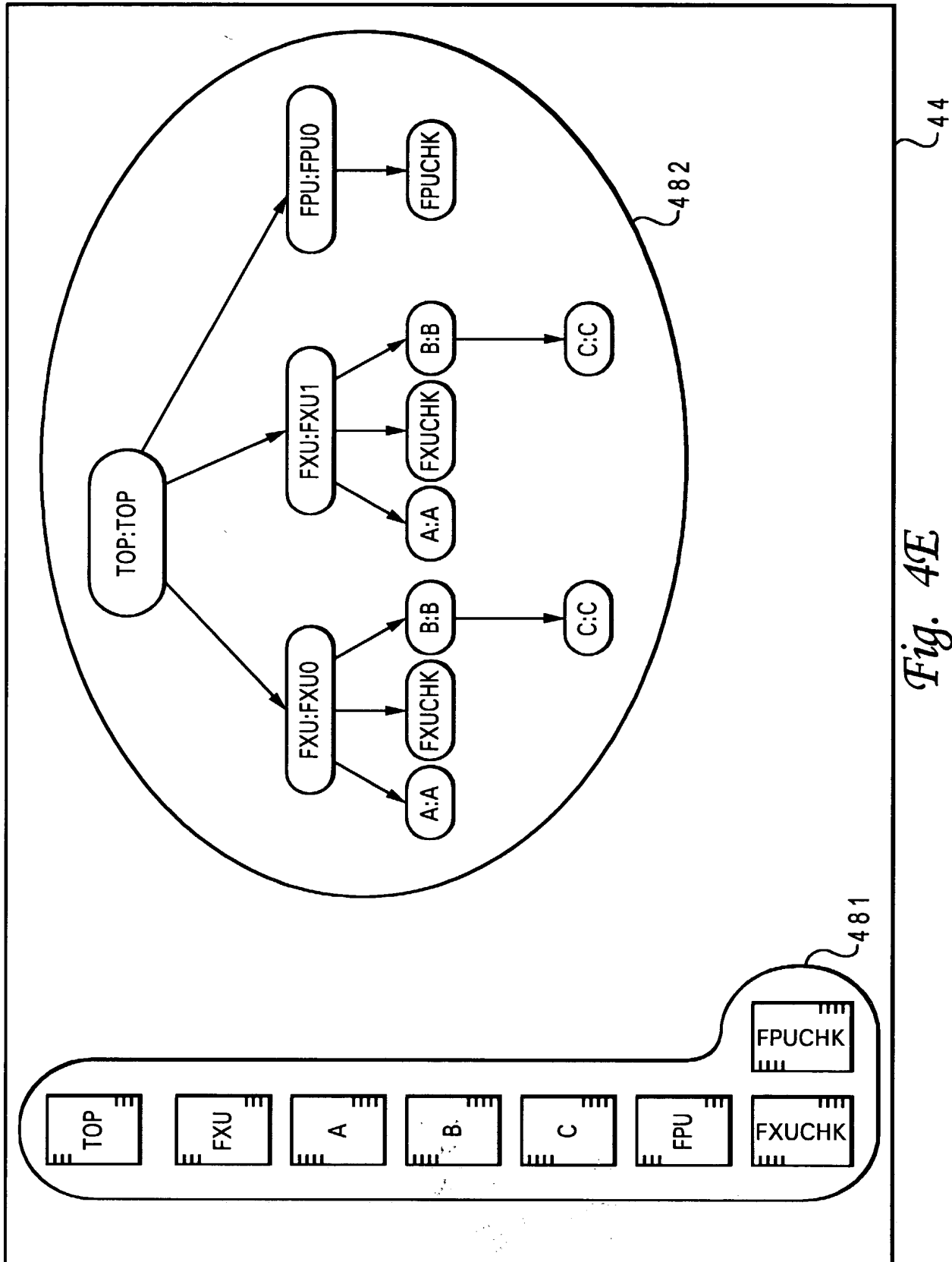


Fig. 4E

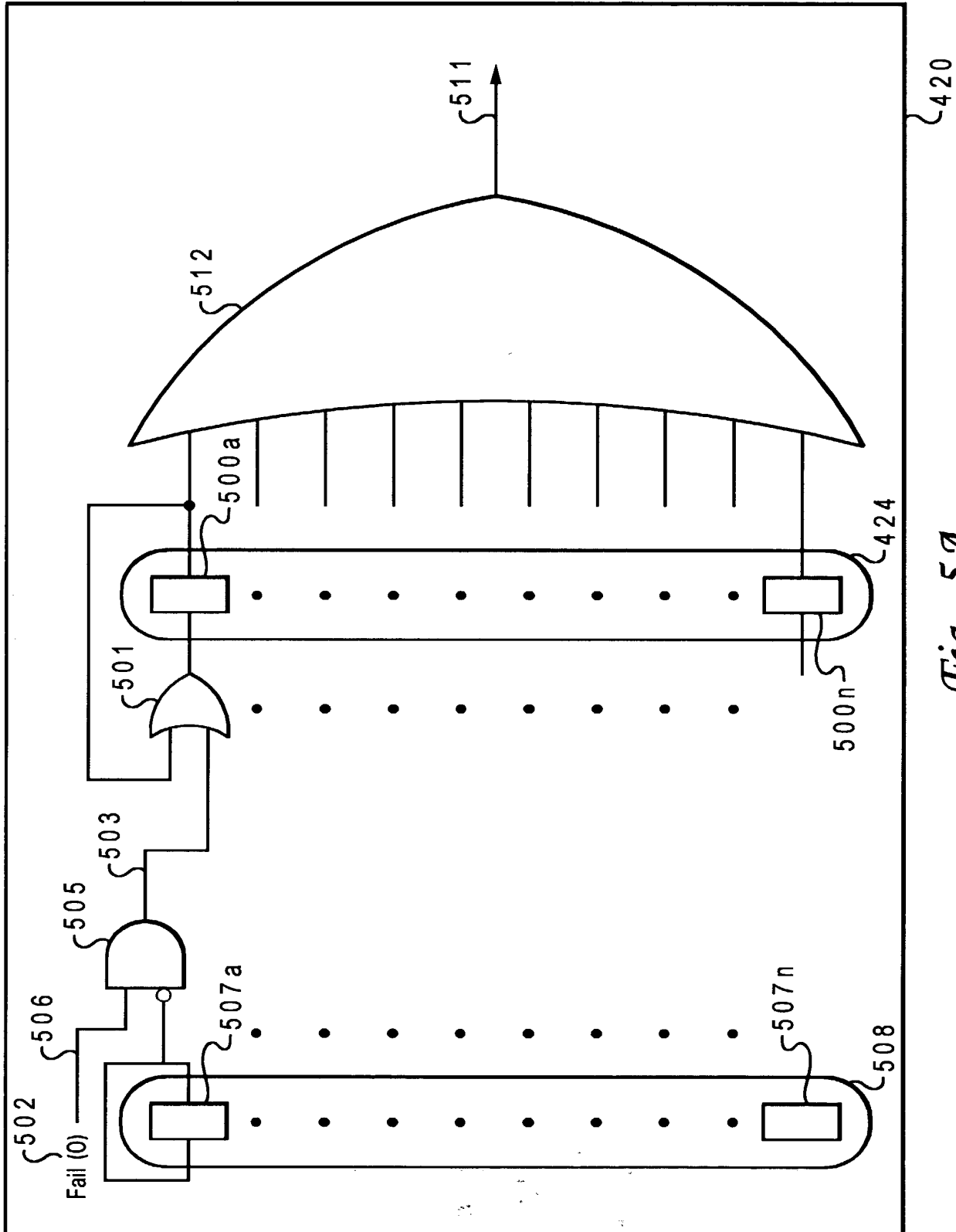


Fig. 5A

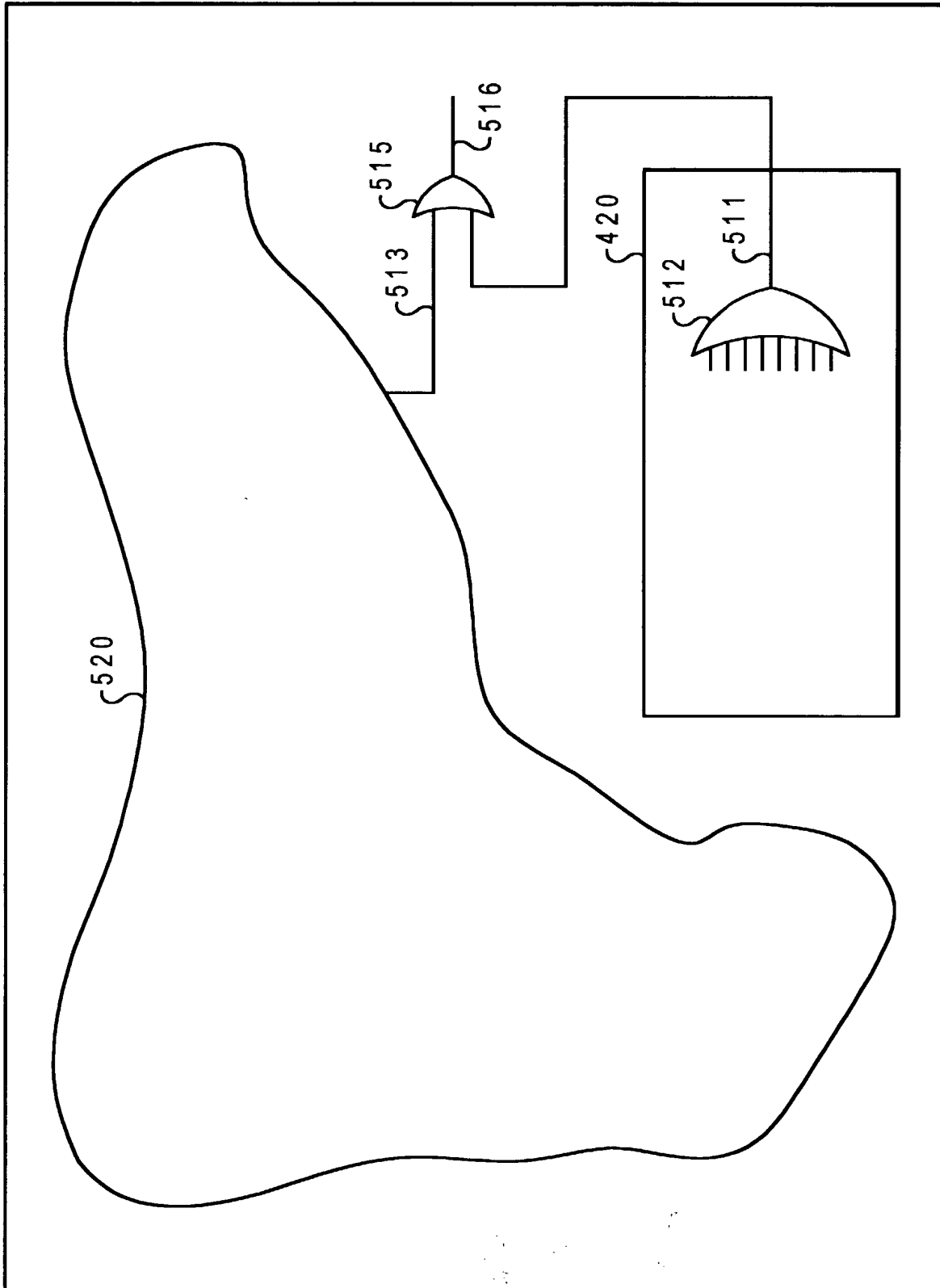


Fig. 5B

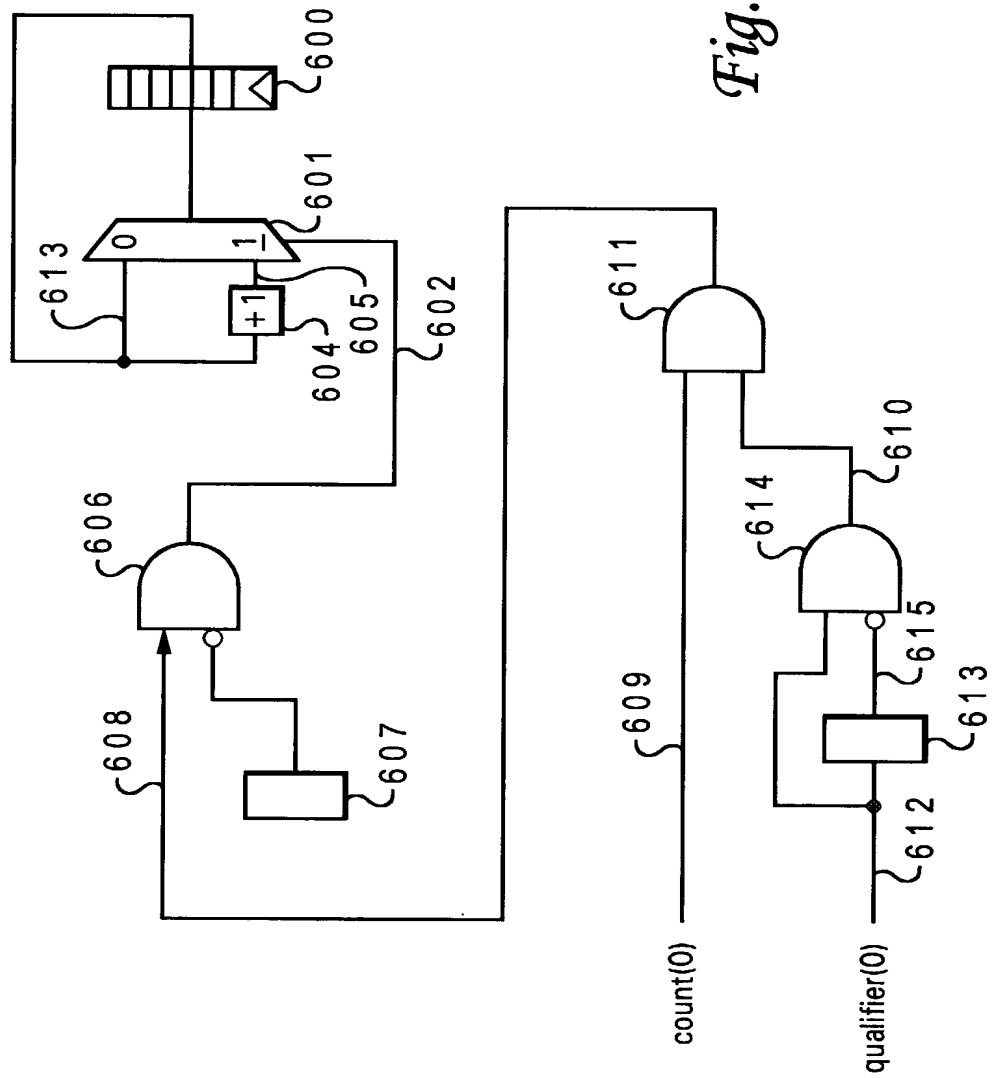


Fig. 6A

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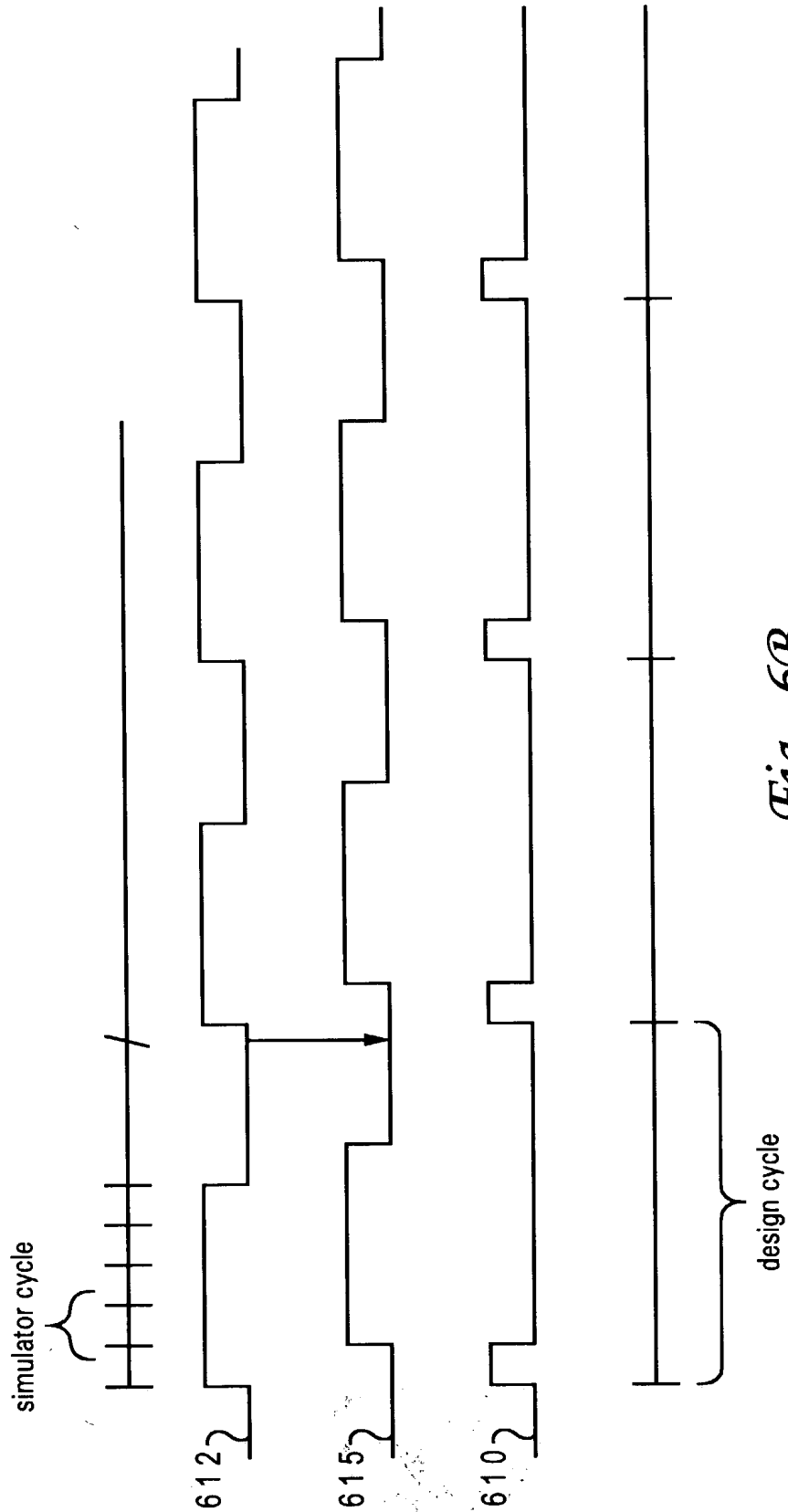


Fig. 6B

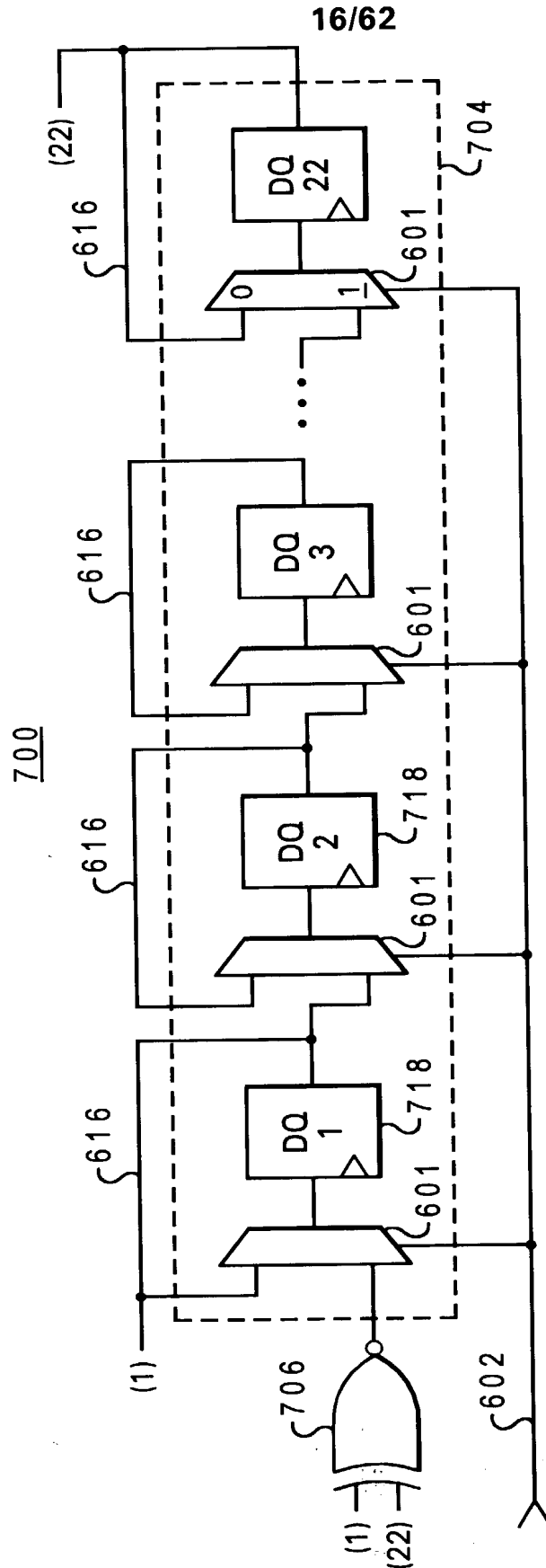


Fig. 7

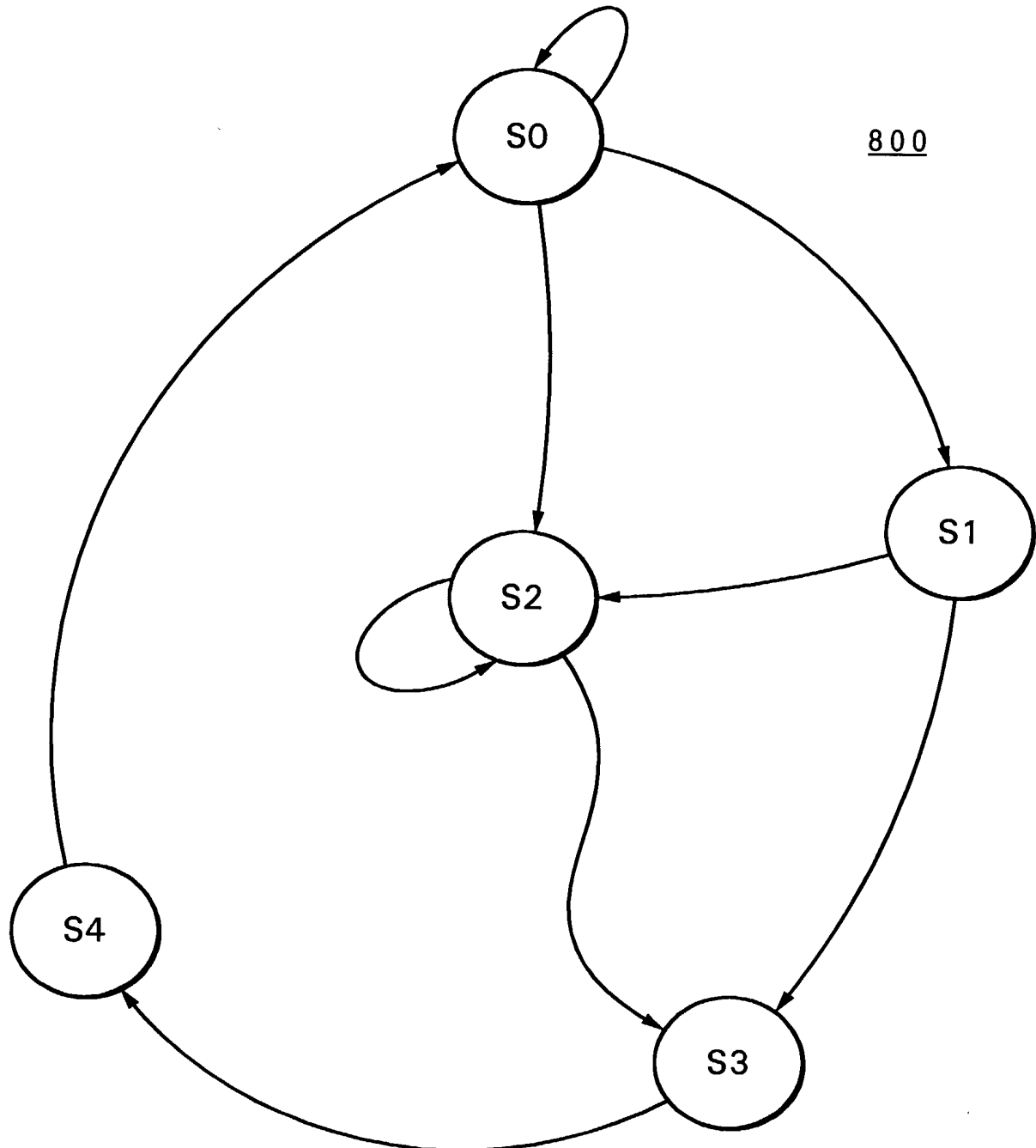


Fig. 8A

Prior Art

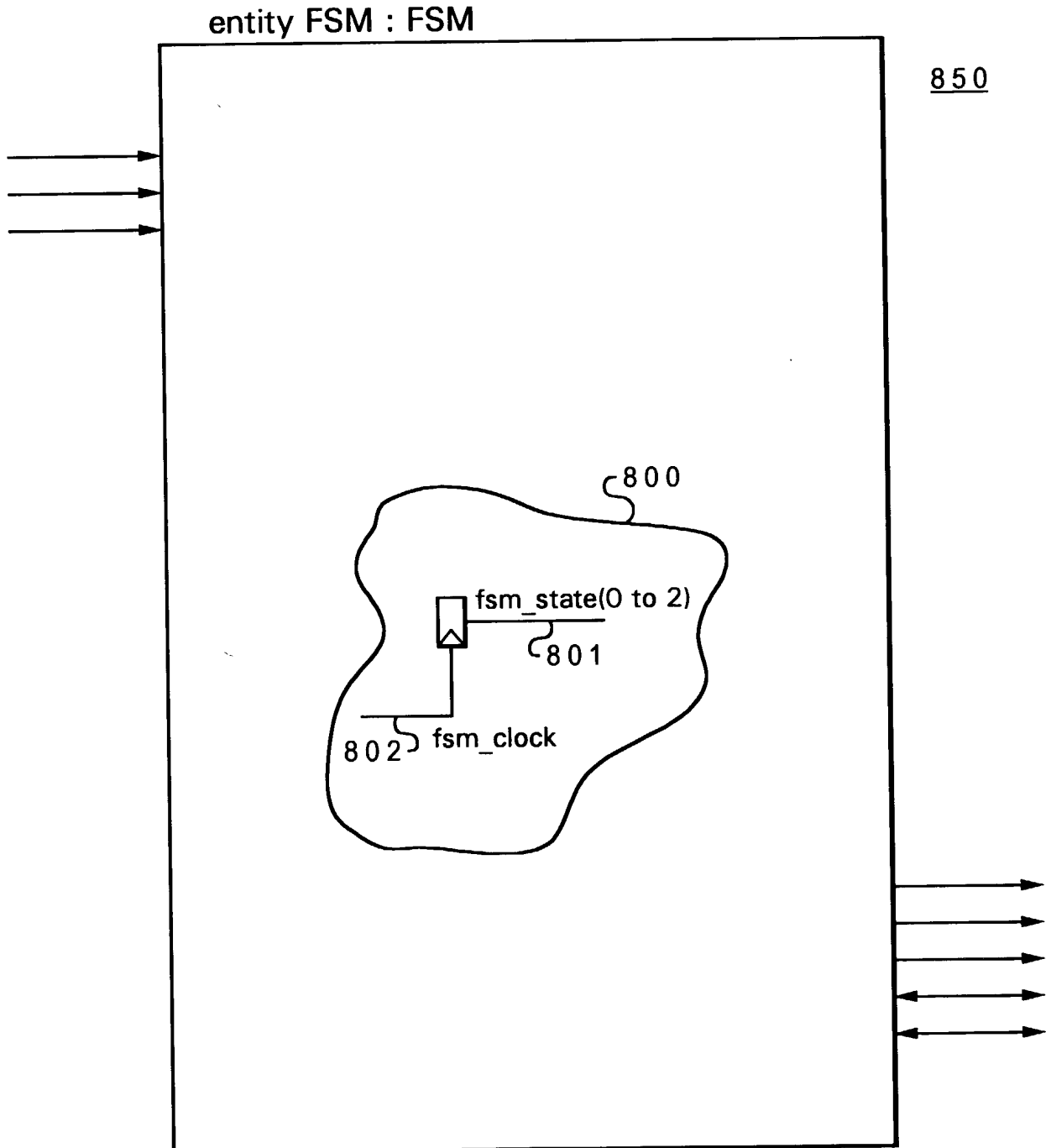


Fig. 8B
Prior Art

ENTITY FSM IS

PORT(
....ports for entity fsm....
);

ARCHITECTURE FSM OF FSM IS

BEGIN

... HDL code for FSM and rest of the entity ...

fsm_state(0 to 2) <= ... Signal 801 ...

8 5 3 {	--!! Embedded FSM : examplefsm;	} 8 5 2	} 8 6 0
8 5 9 {	--!! clock : (fsm_clock);		
8 5 4 {	--!! state_vector : (fsm_state(0 to 2));		
8 5 5 {	--!! states : (S0, S1, S2, S3, S4);		
8 5 6 {	--!! state_encoding : ('000', '001', '010', '011', '100');		
8 5 7 {	--!! arcs : (S0 => S0, S0 => S1, S0 => S2,		
	--!! (S1 => S2, S1 => S3, S2 => S2,		
	--!! (S2 => S3, S3 => S4, S4 => S0);		
8 5 8 {	--!! End FSM;		

END;

Fig. 8C

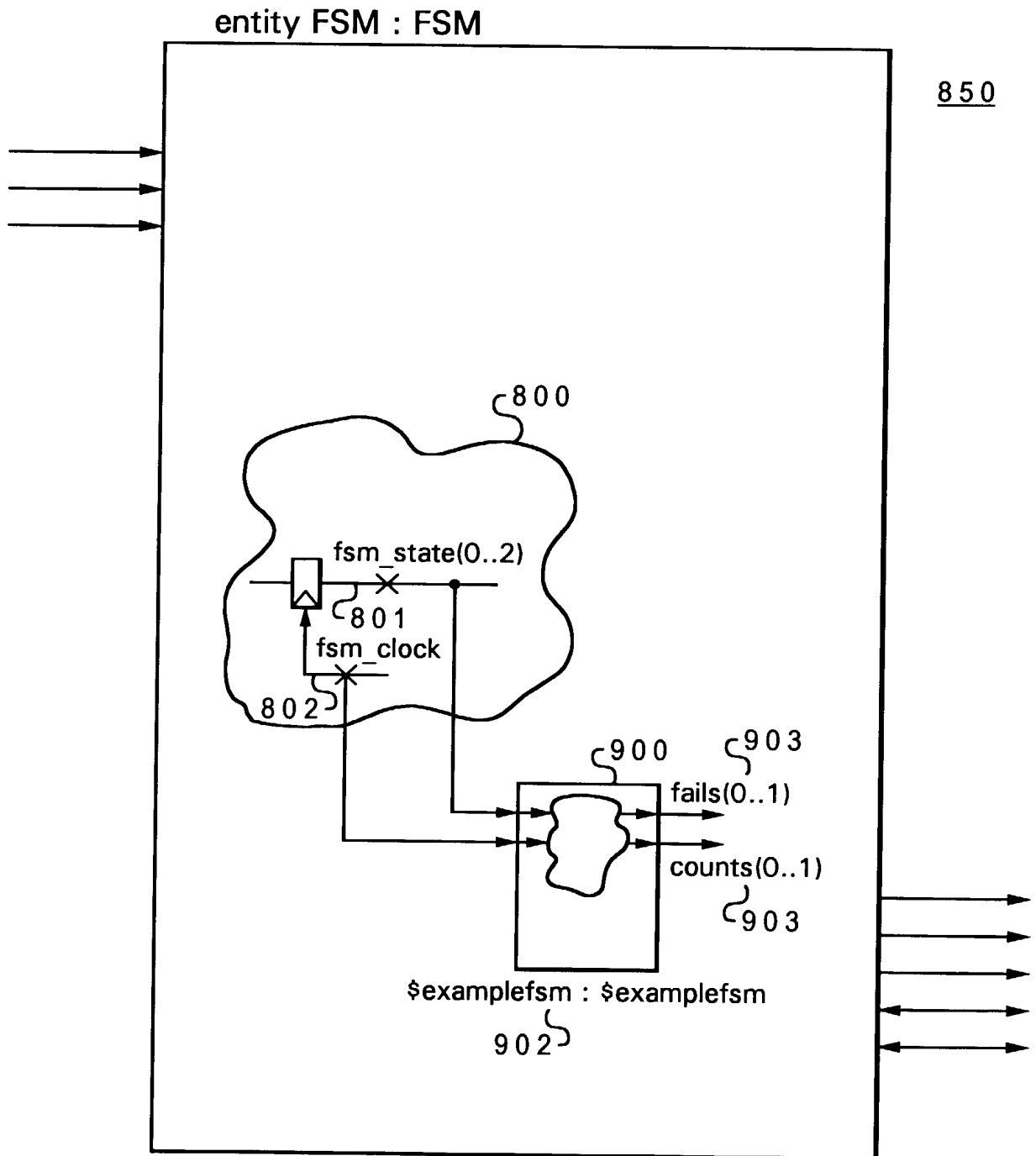
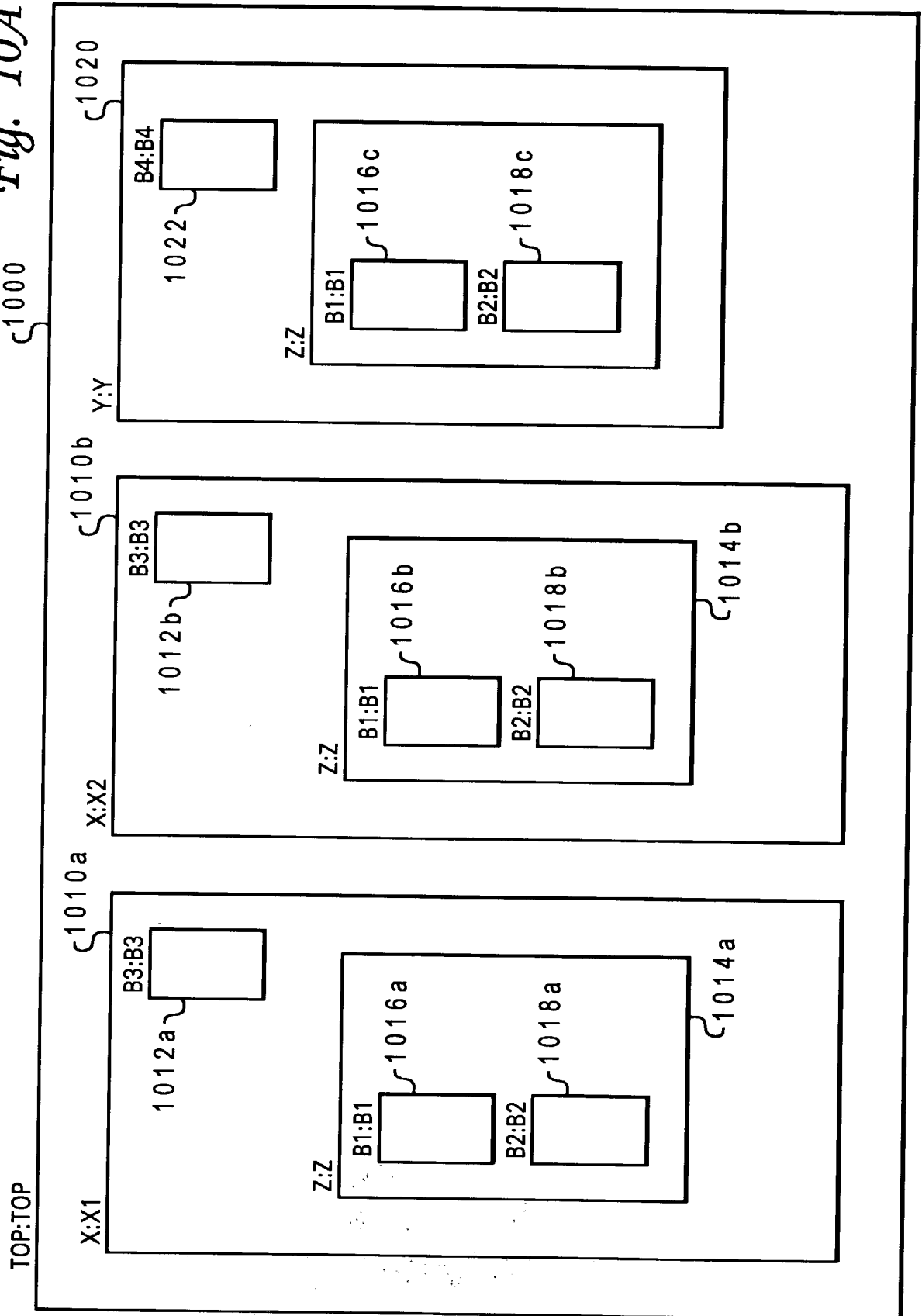


Fig. 9

Fig. 10A



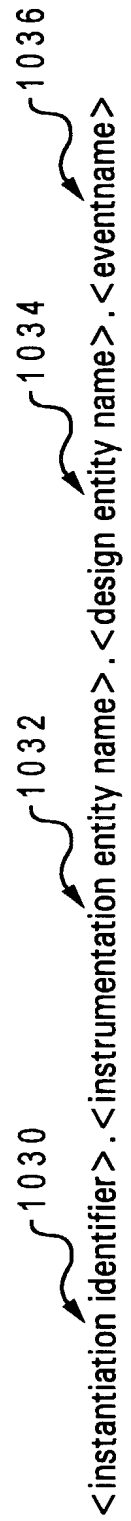


Fig. 10B

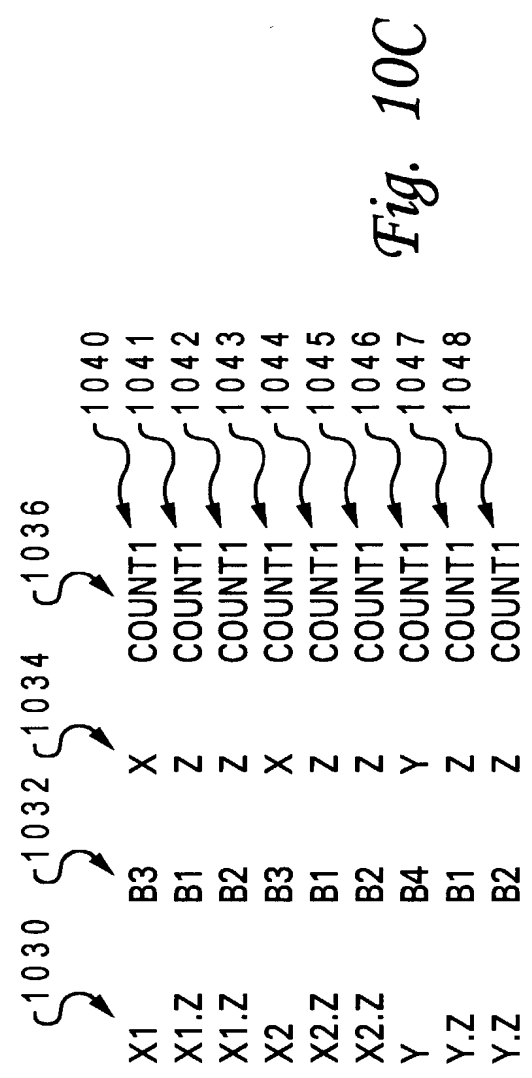


Fig. 10C

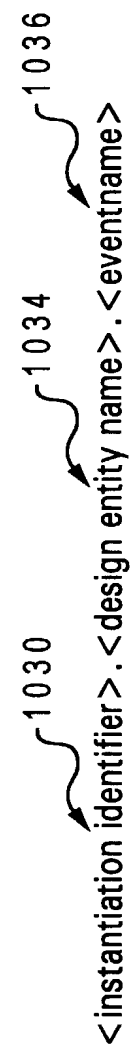
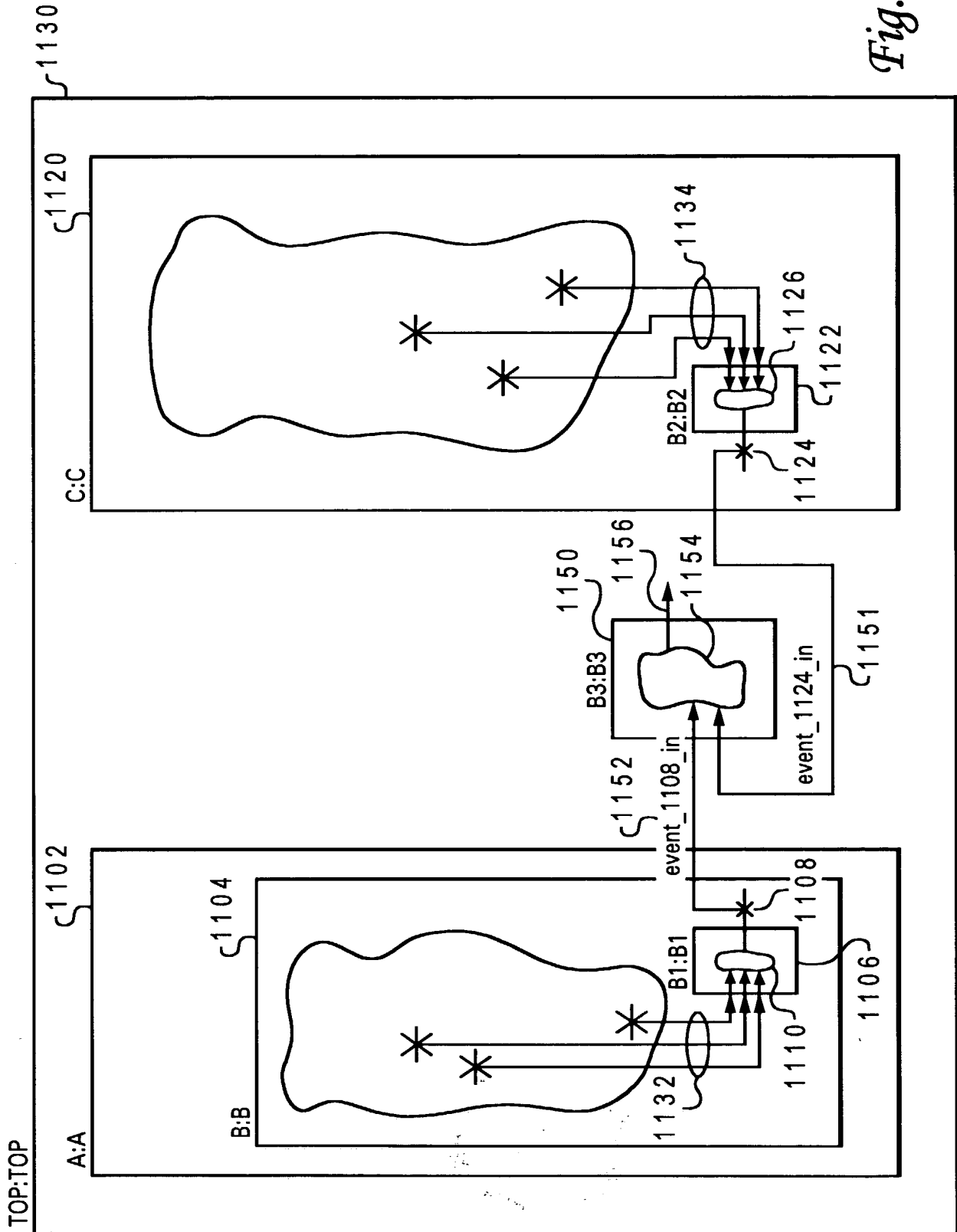


Fig. 10D

Fig. 11A



```

--!! Inputs
--!! event_1108_in <= C.[B2.count.event_1108];
--!! event_1124_in <= A.B.[B1.count.event_1124];
--!! End Inputs

```

Diagram annotations for Fig. 11B:

- 1163: bracket above "C.[B2.count.event_1108]"
- 1165: bracket above "A.B.[B1.count.event_1124]"
- 1161: bracket above "C.[B2.count.event_1108]"
- 1162: bracket above "A.B.[B1.count.event_1124]"
- 1164: bracket below "C.[B2.count.event_1108]"
- 1166: bracket below "A.B.[B1.count.event_1124]"

Fig. 11B

```

--!! Inputs
--!! event_1108_in <= C.[count.event_1108];
--!! event_1124_in <= B.[count.event_1124];
--!! End Inputs

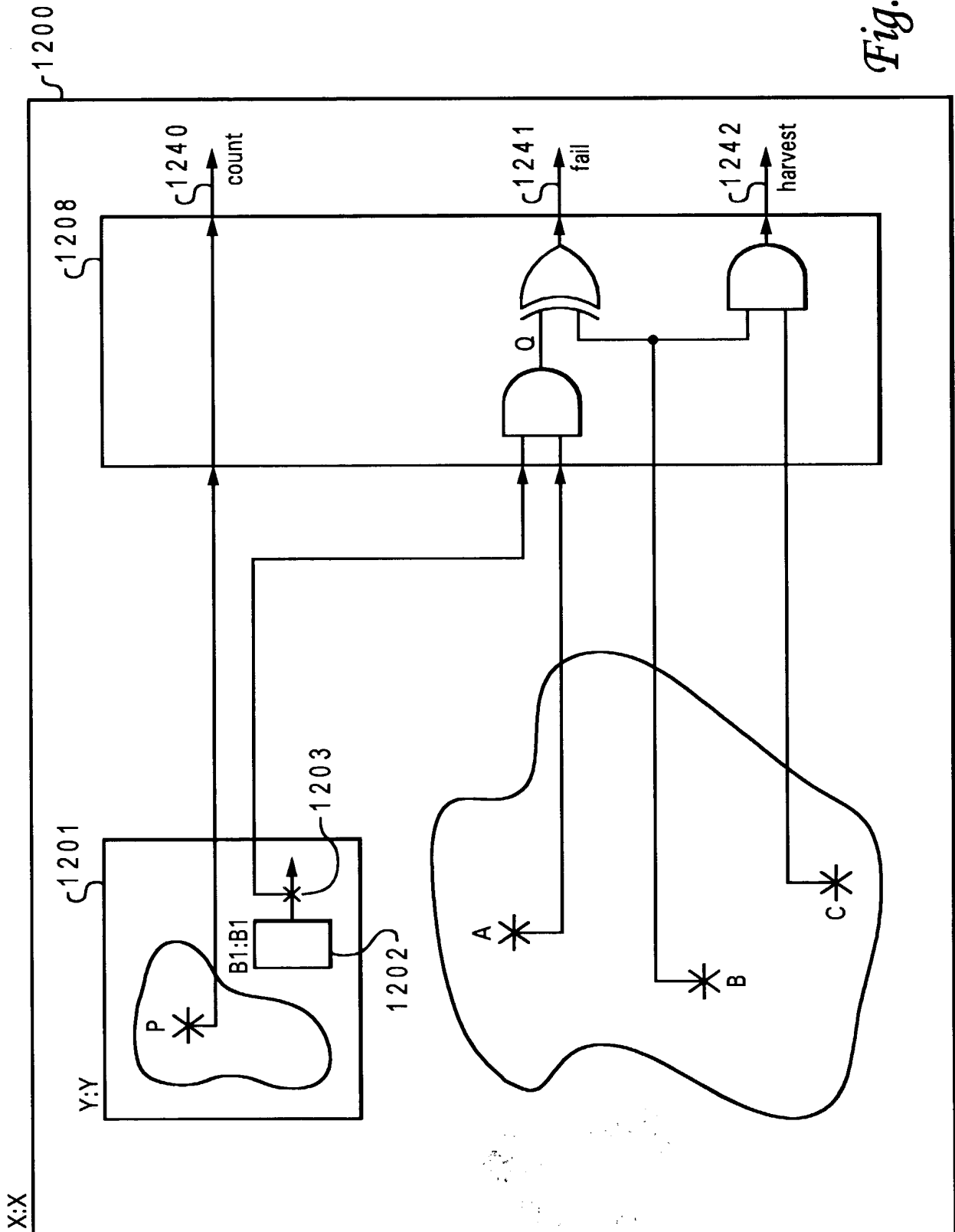
```

Diagram annotations for Fig. 11C:

- 1171: bracket above "C.[count.event_1108]"
- 1172: bracket above "B.[count.event_1124]"

Fig. 11C

Fig. 12A



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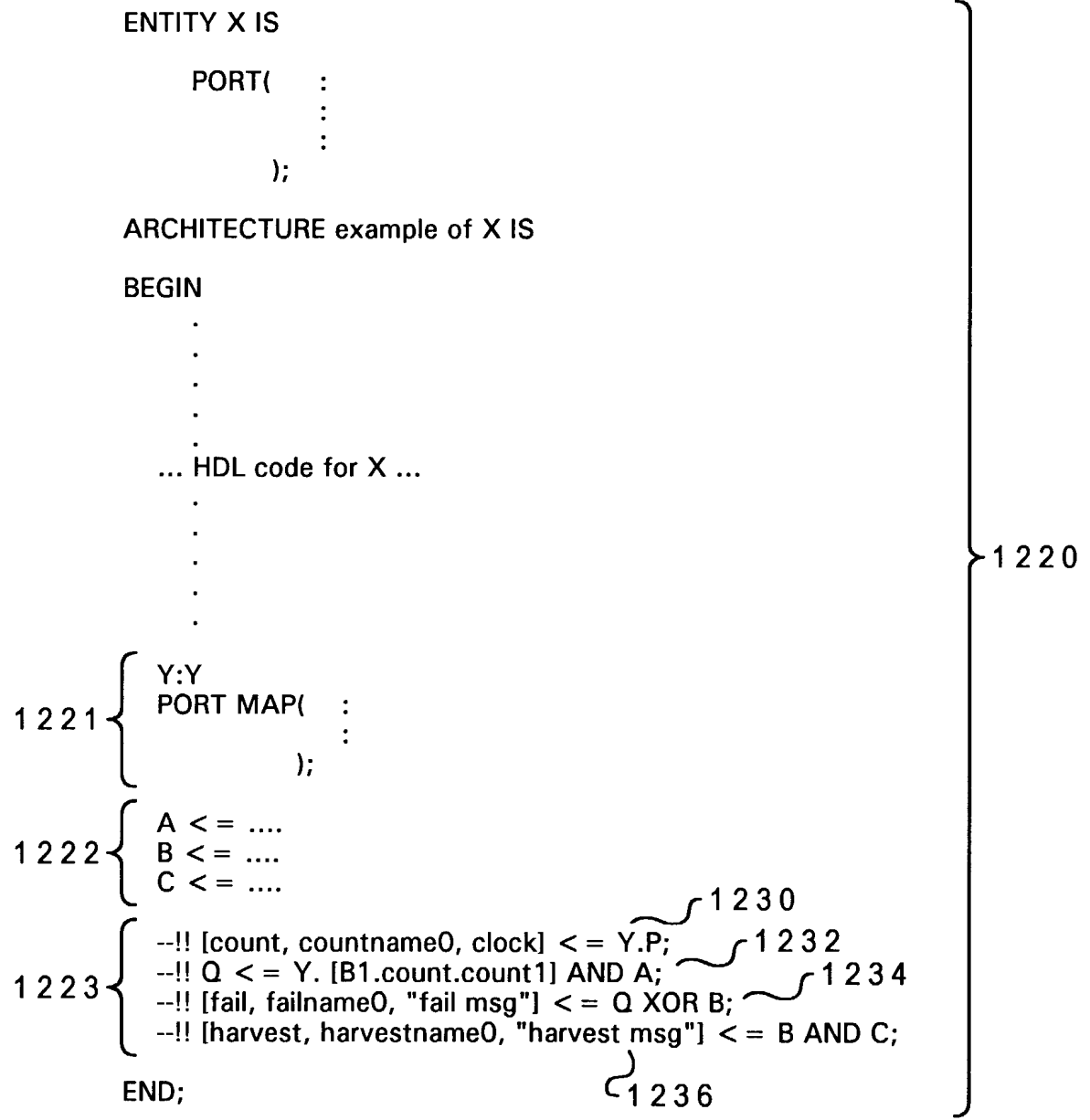


Fig. 12B

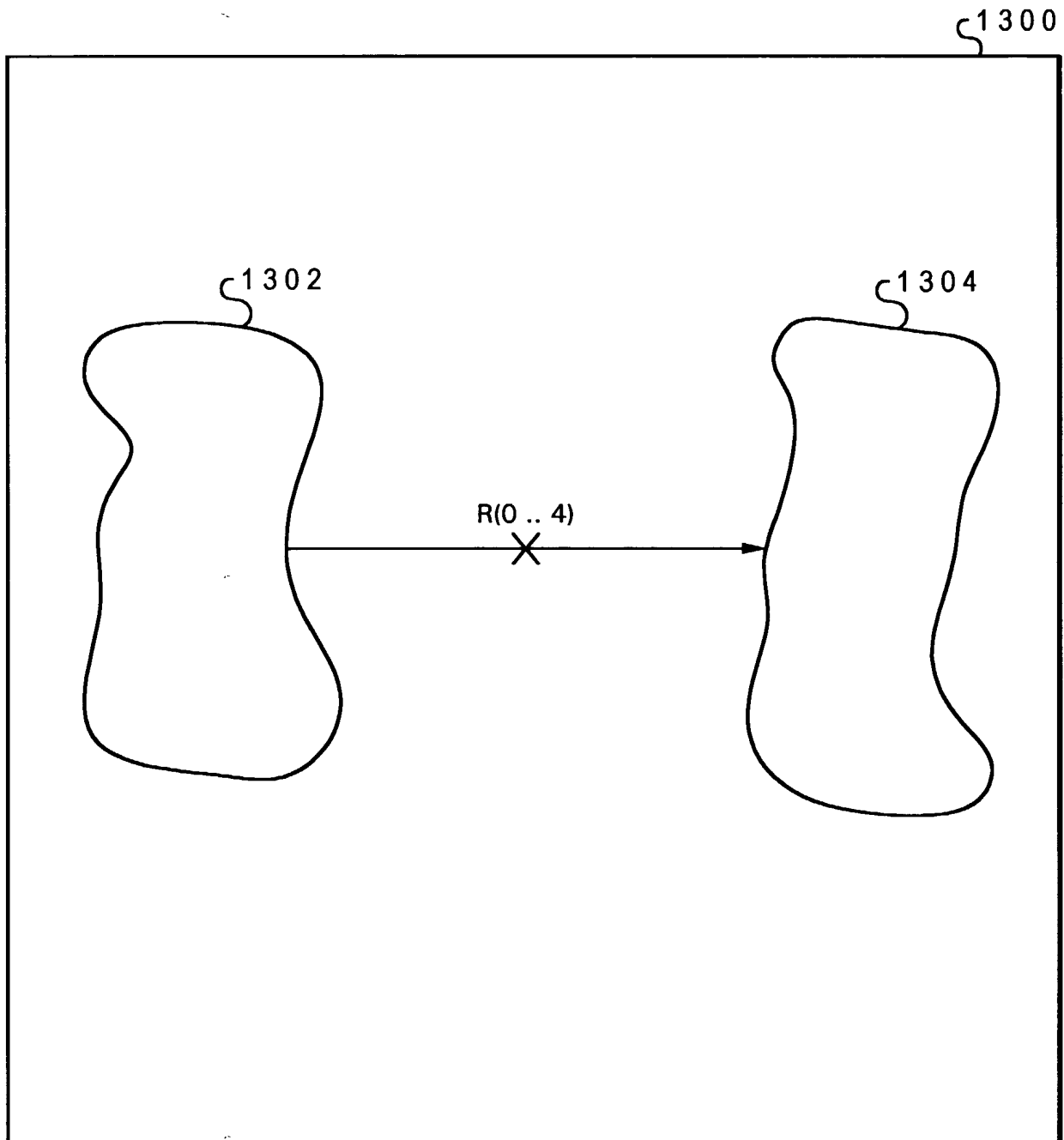
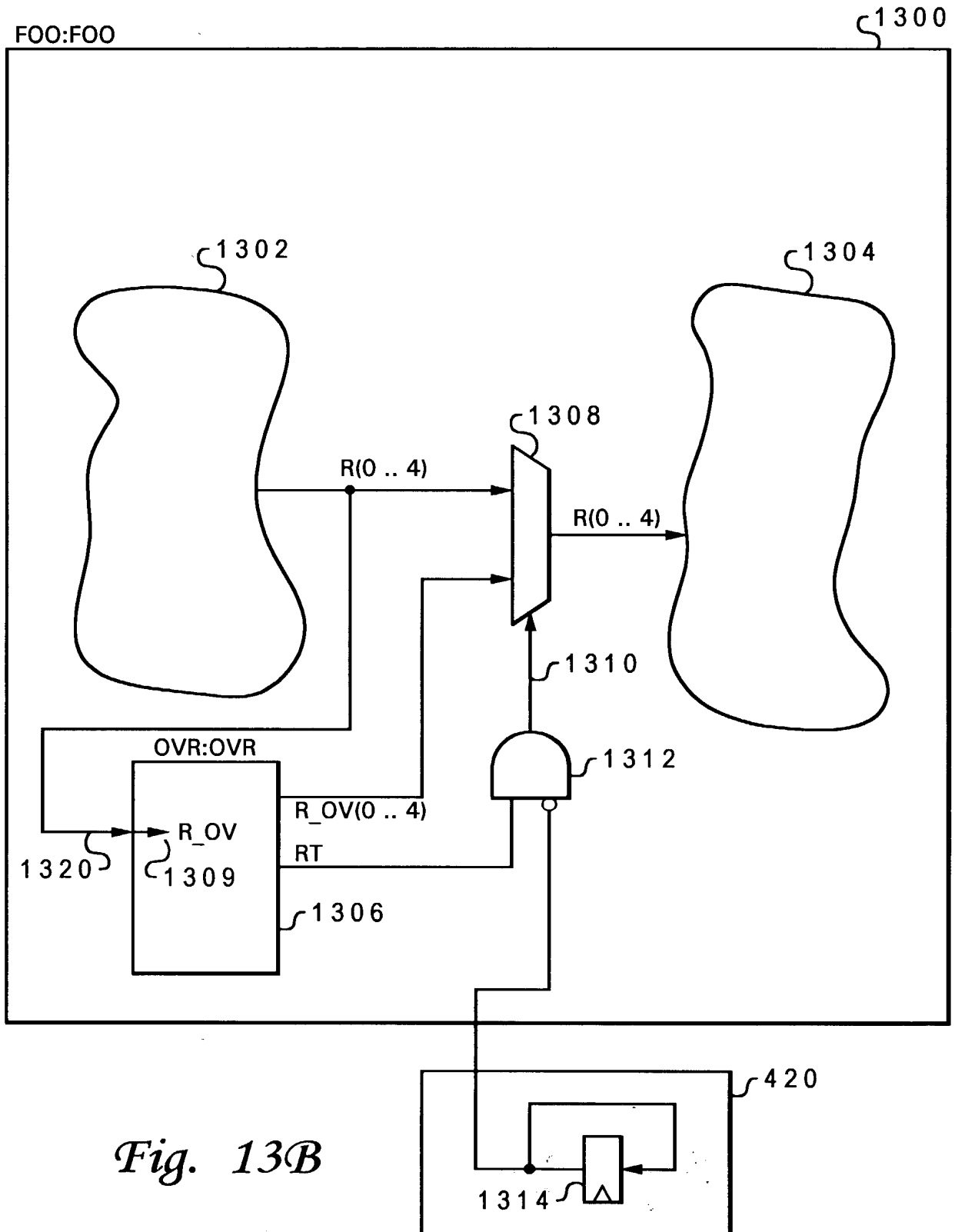


Fig. 13A



```

ENTITY OVR IS
    PORT( R_IN      : IN std_ulogic_vector(0 .. 4);
          .
          .
          ... other ports as required ...
          .
          .
          R_OV      : OUT std_ulogic_vector(0 .. 4);
          RT         : OUT std_ulogic
    );

--!! BEGIN
--!! Design Entity: FOO;

--!! Inputs (0 to 4)
--!! R_IN => {R(0 .. 4)};
--!! :
--!! ... other ports as needed ...
--!! :
--!! End Inputs

--!! Outputs
--!! <R_OVRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];
--!! End Outputs

--!! End

ARCHITECTURE example of OVR IS
BEGIN
    ... HDL code for entity body section ...
END;
    
```

Diagram annotations (brackets and labels):

- 1364: Brackets the input port `R_IN`.
- 1362: Brackets the output port `R_OV`.
- 1363: Brackets the output port `RT`.
- 1360: Brackets the input assignment `R_IN => {R(0 .. 4)}`.
- 1361: Brackets the output assignment `R_OV(0 .. 4) => R(0 .. 4) [RT]`.
- 1356: Brackets the output assignment block.
- 1351: Brackets the input and output assignment blocks.
- 1340: Brackets the entire entity definition.
- 1358: Brackets the architecture body section.

Fig. 13C

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ENTITY FOO IS

PORT(:
:
:
);

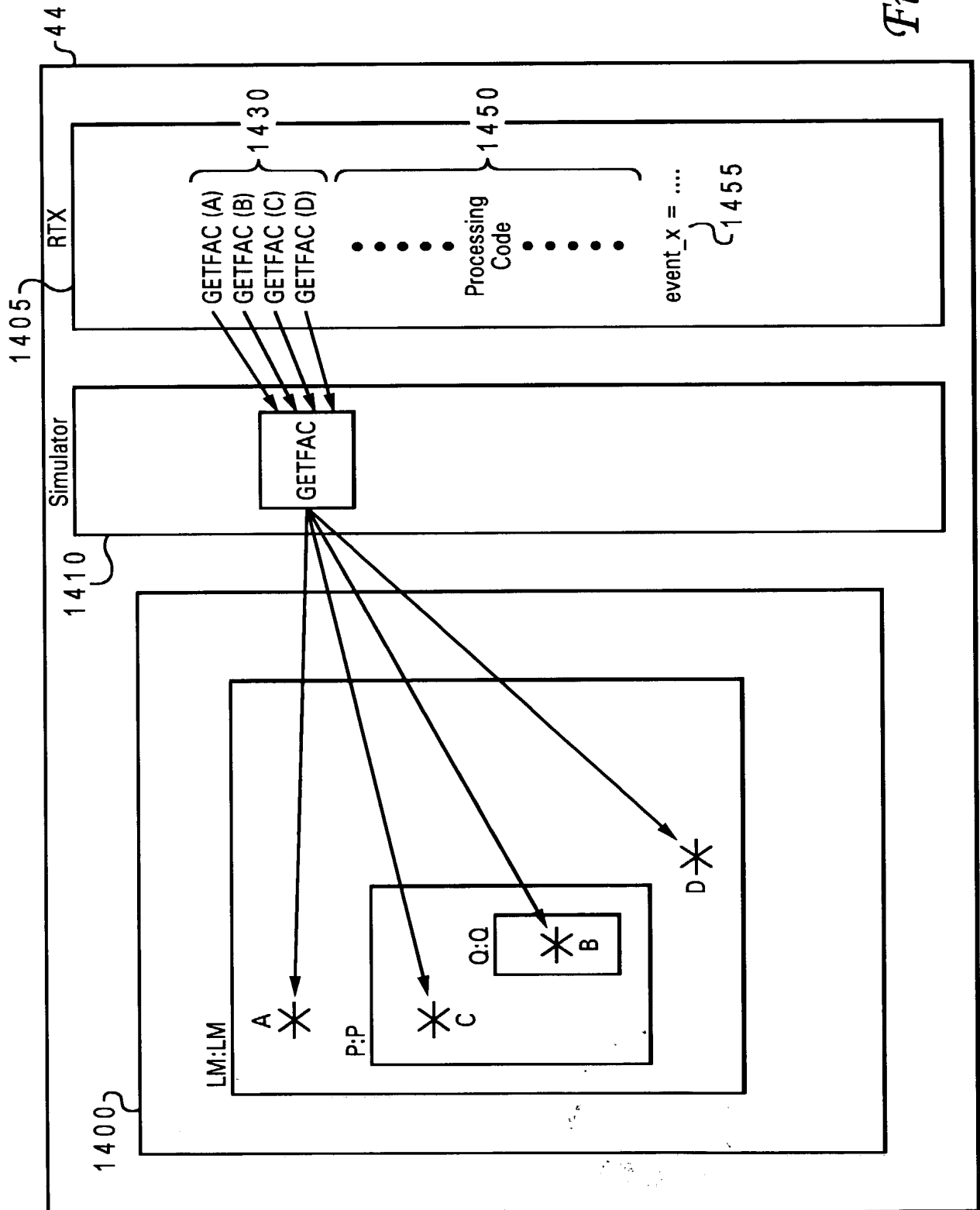
ARCHITECTURE example of FOO IS

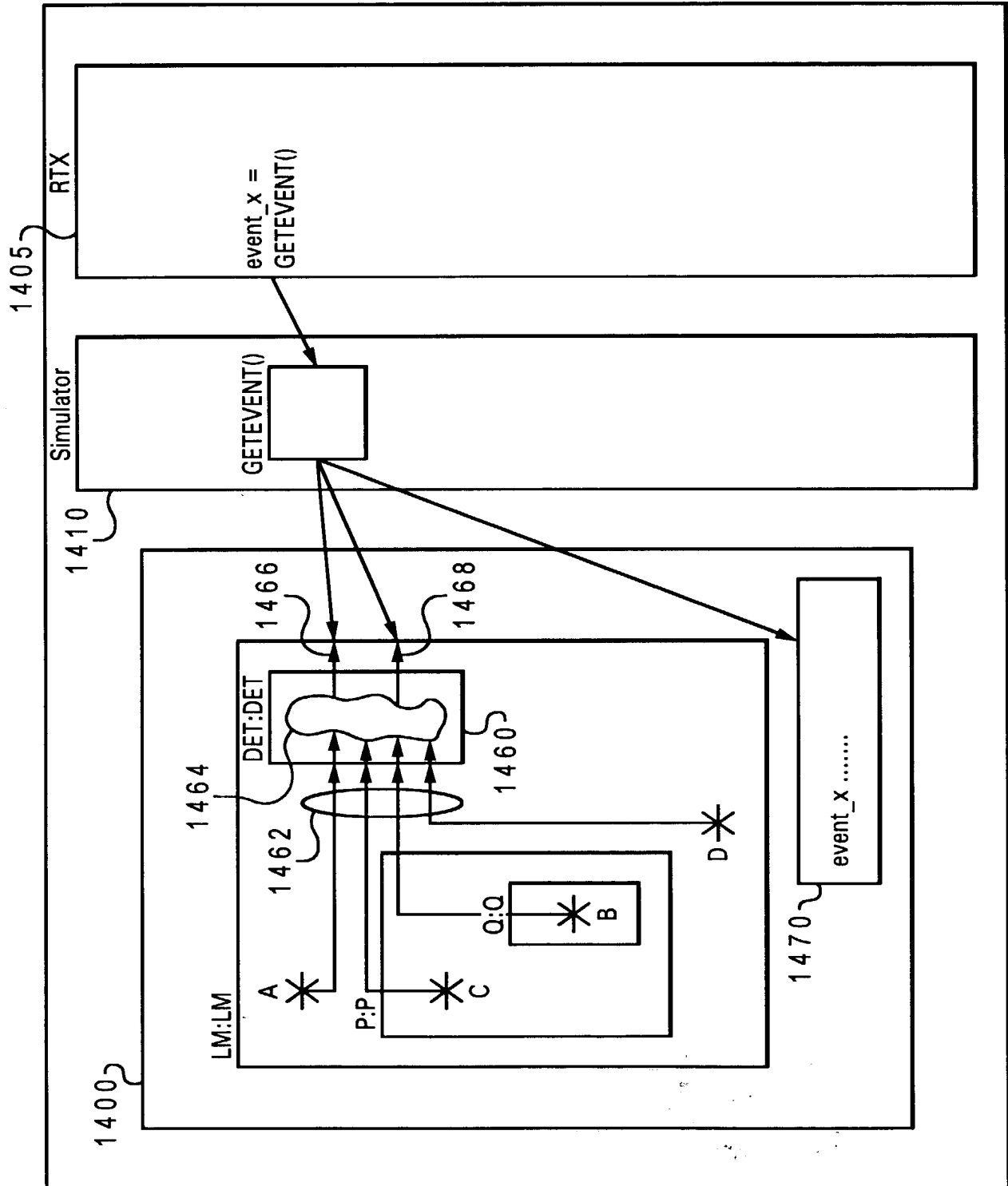
BEGIN

.
.
.
.
.
R <=
.
.
.
.

1380 { --!! R_IN <= {R}; 1381
--!! 1382
--!!
--!! R_OV(0 to 4) <=; 1383
--!! RT <=;
--!! [override, R_OVRIDE, R(0 .. 4), RT] <= R_OV(0 to 4); 1384

Fig. 13D





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```

ENTITY DET IS
    PORT(
        A      : IN std_ulogic;
        B      : IN std_ulogic_vector(0 to 5);
        C      : IN std_ulogic;
        D      : IN std_ulogic;
        :
        :
        event_x : OUT std_ulogic_vector(0 to 2);
        x_here  : OUT std_ulogic;
    );

    --!! BEGIN
    --!! Design Entity: LM;

    --!! Inputs
    --!! A    => A;
    --!! B    => P.Q.B;
    --!! C    => P.C;
    --!! D    => D;
    --!! End Inputs

    --!! Detections
    --!! <event_x>:event_x(0 to 2) [x_here];
    --!! End Detections

    --!! End;

    ARCHITECTURE example of DET IS
    BEGIN
        ... HDL code ...

    END;
    
```

1491 {

1493 {

1495 {

1494 {

1480 {

1492 {

Fig. 14C

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1660

1661

1662

1663

1:

X1

B3

X

COUNT1

2:

X1.Z

B1

Z

COUNT1

3:

X1.Z

B2

Z

COUNT1

4:

X2

B3

X

COUNT1

5:

X2.Z

B1

Z

COUNT1

6:

X2.Z

B2

Z

COUNT1

7:

Y

B4

Y

COUNT1

8:

Y.Z

B1

Z

COUNT1

9:

Y.Z

B2

Z

COUNT1

Fig. 15

1601

Fig. 16A is a network diagram illustrating a Wide Area Network (WAN) 1690 connected to four separate Local Networks (1680a, 1680b, 1680c, 1680d). Each Local Network is represented by a dashed oval and contains a central 'Local Network' (1610a, 1610b, 1610c, 1610d) and various devices (1600a, 1600b, 1600n, 1607, 1604). The WAN 1690 is represented by a central oval. The diagram shows the following components and connections:

- Local Network 1680a:** Contains a 'Local Network' 1610a connected to devices 1600a, 1600b, 1600n, and 1607. Device 1607 is connected to three devices 1604.
- Local Network 1680b:** Contains a 'Local Network' 1610b connected to devices 1600a, 1600b, and 1600n.
- Local Network 1680c:** Contains a 'Local Network' 1610c connected to devices 1600a, 1600b, and 1600n.
- Local Network 1680d:** Contains a 'Local Network' 1610d connected to devices 1600a, 1600b, and 1600n.
- WAN 1690:** A central oval representing the Wide Area Network, which is connected to all four Local Networks (1680a, 1680b, 1680c, 1680d).

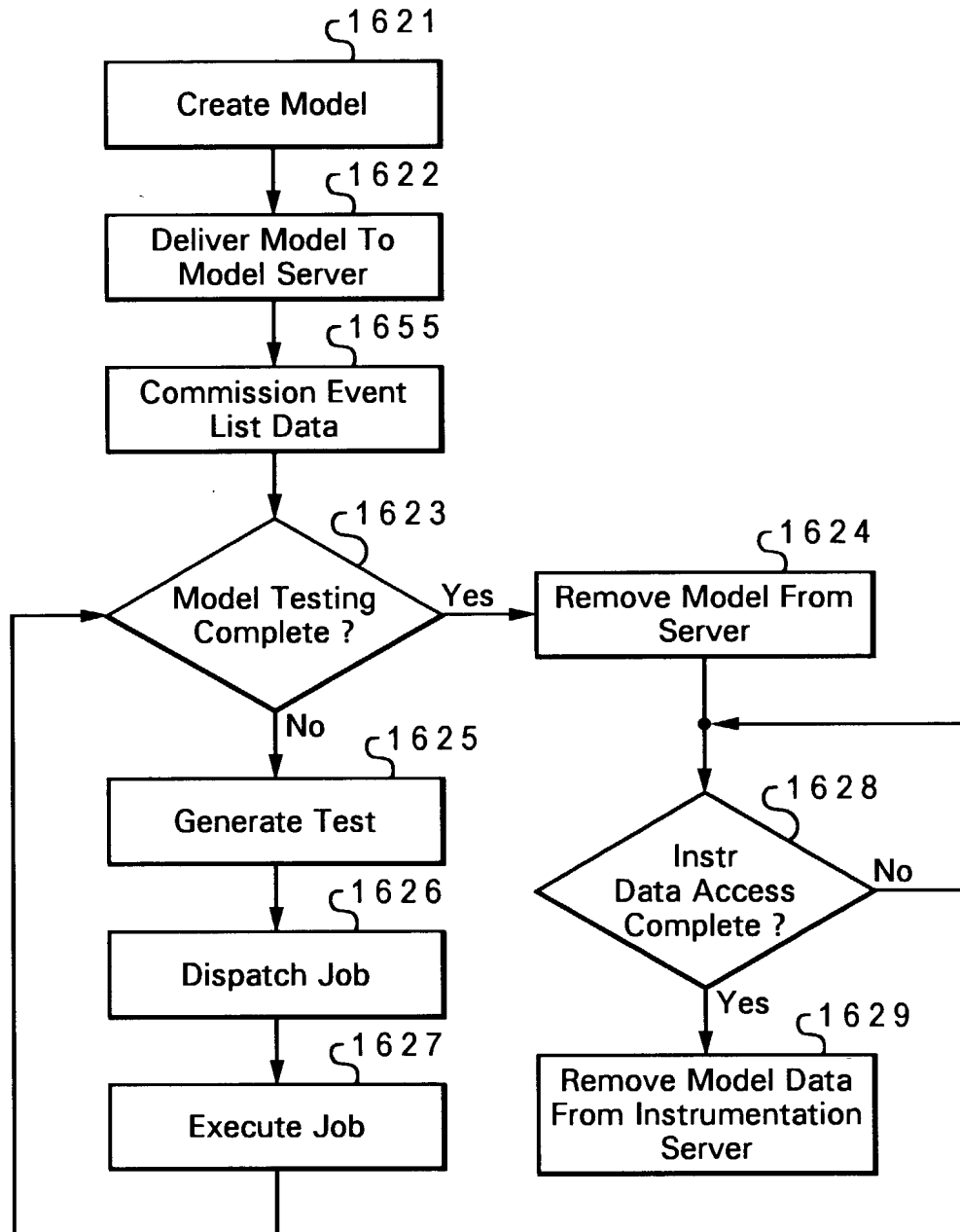


Fig. 16B

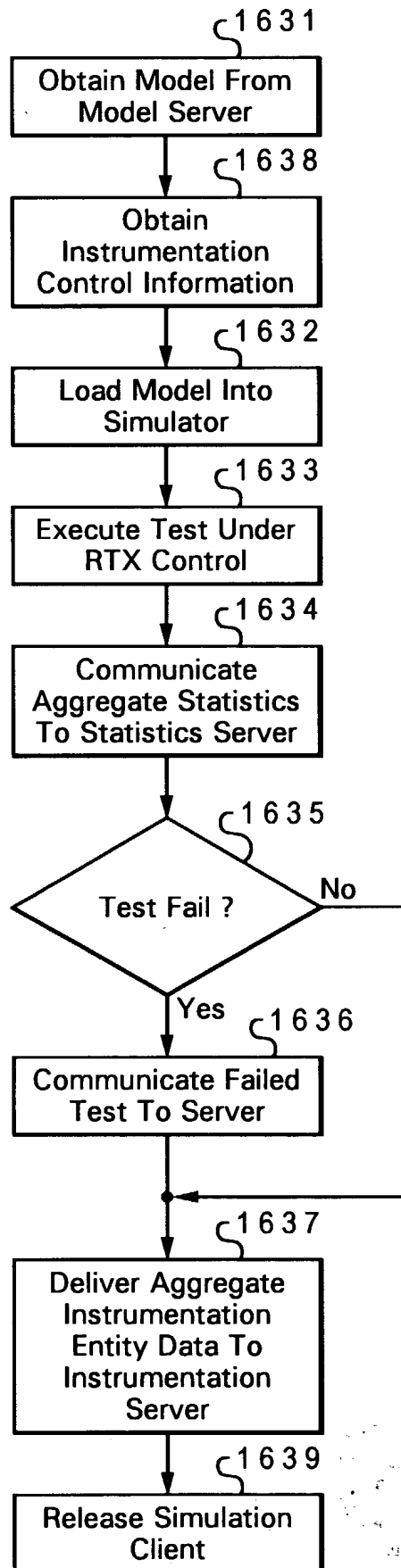


Fig. 16C

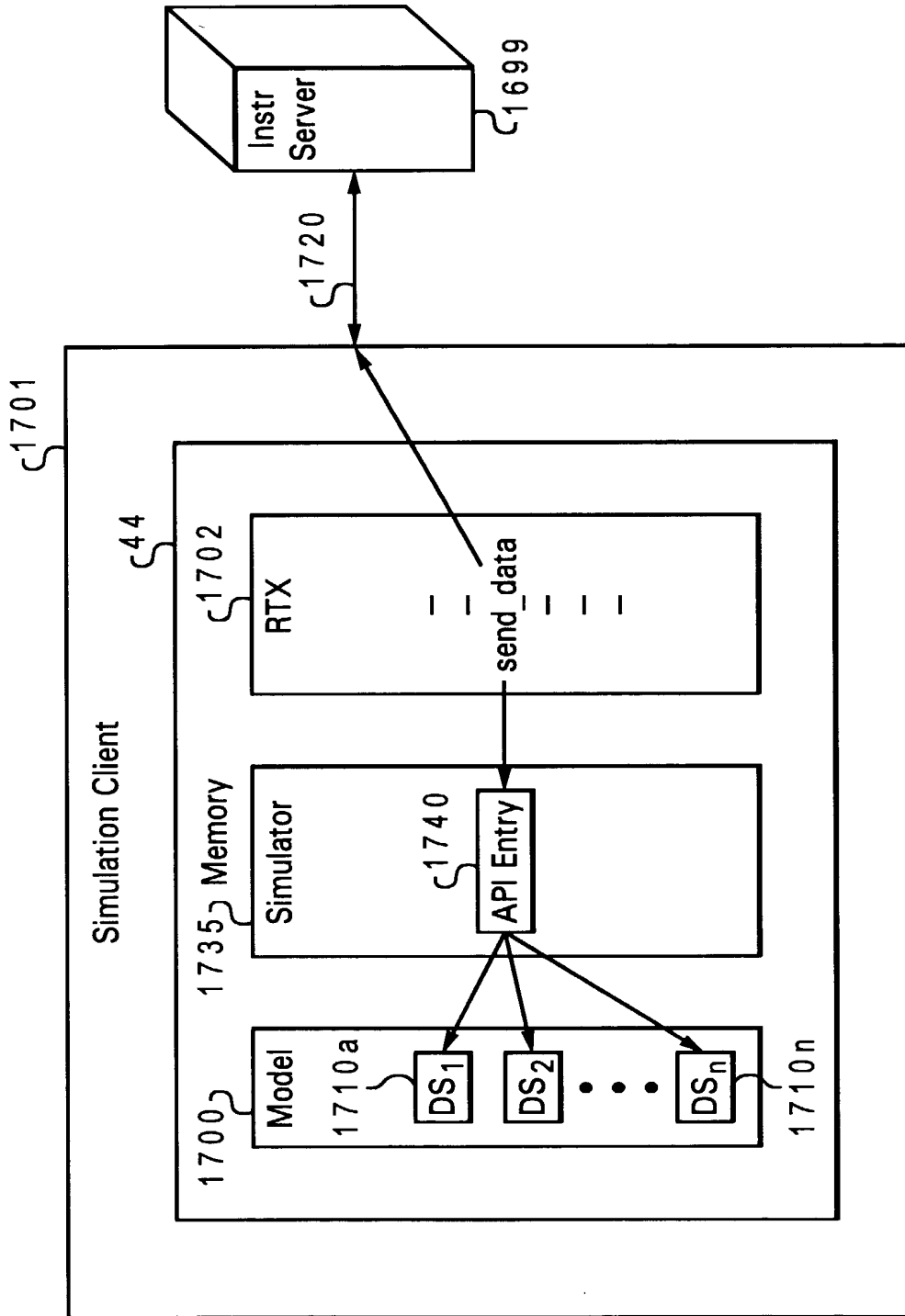


Fig. 17A

Fig. 17B

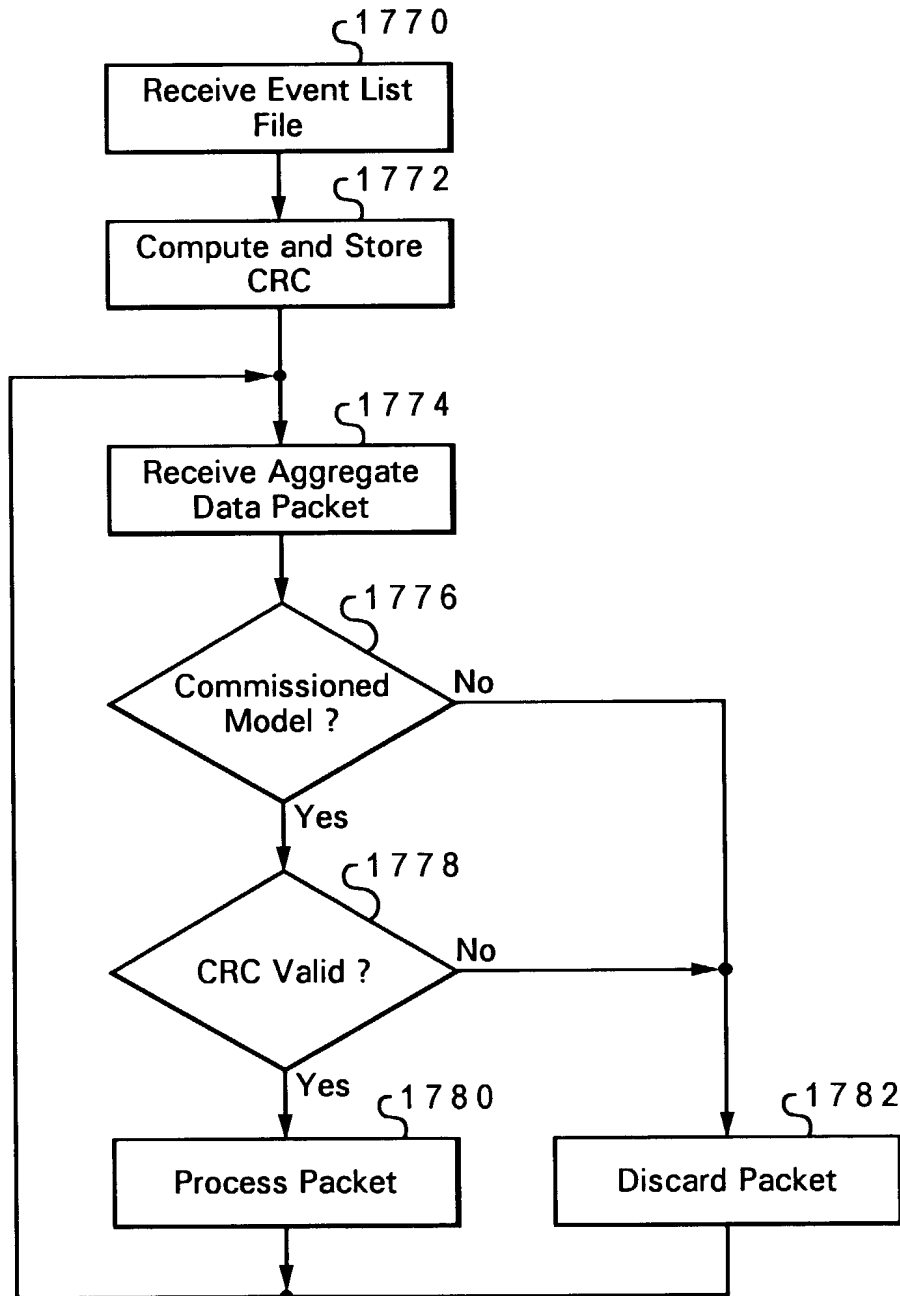


Fig. 17C

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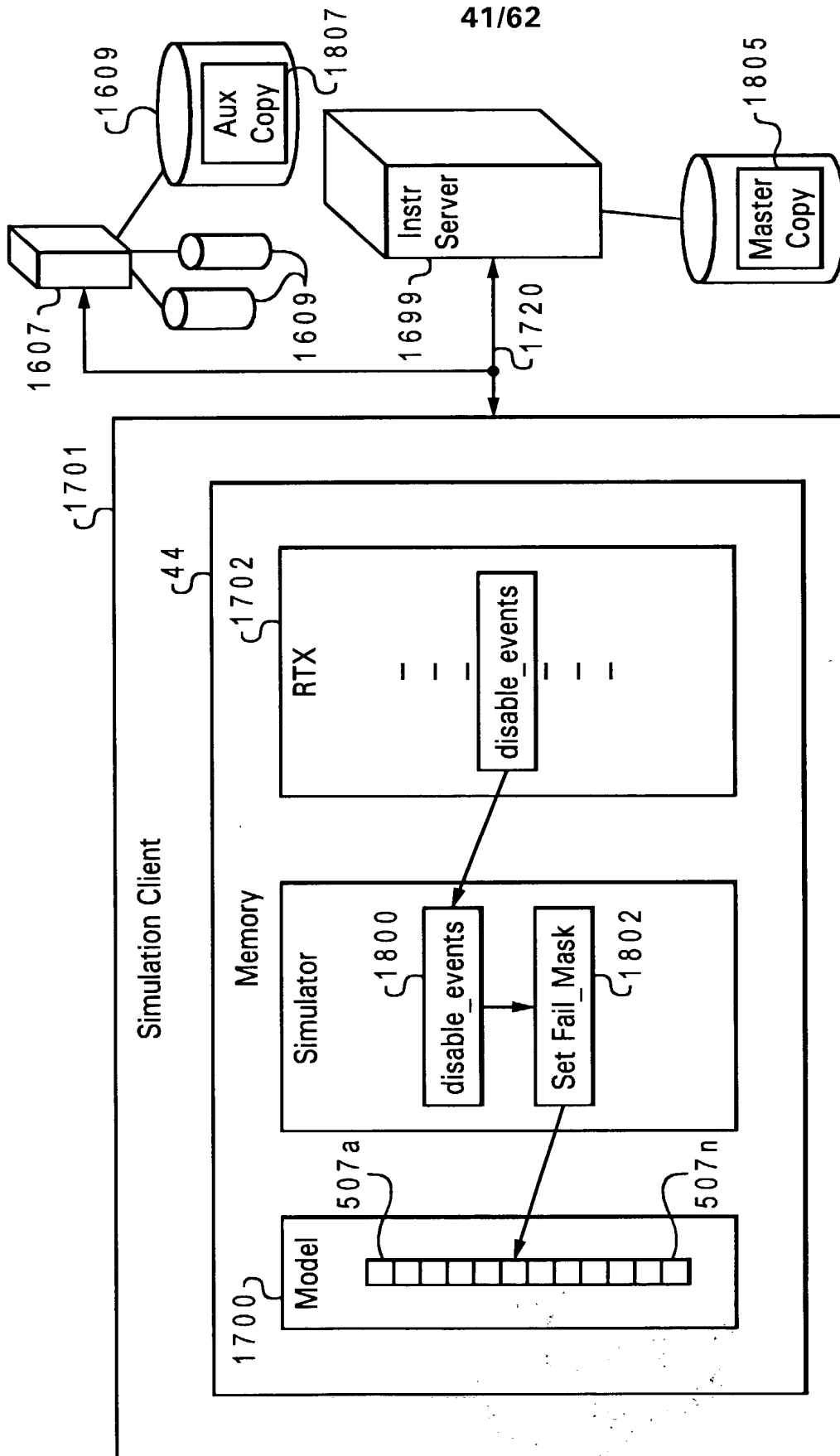
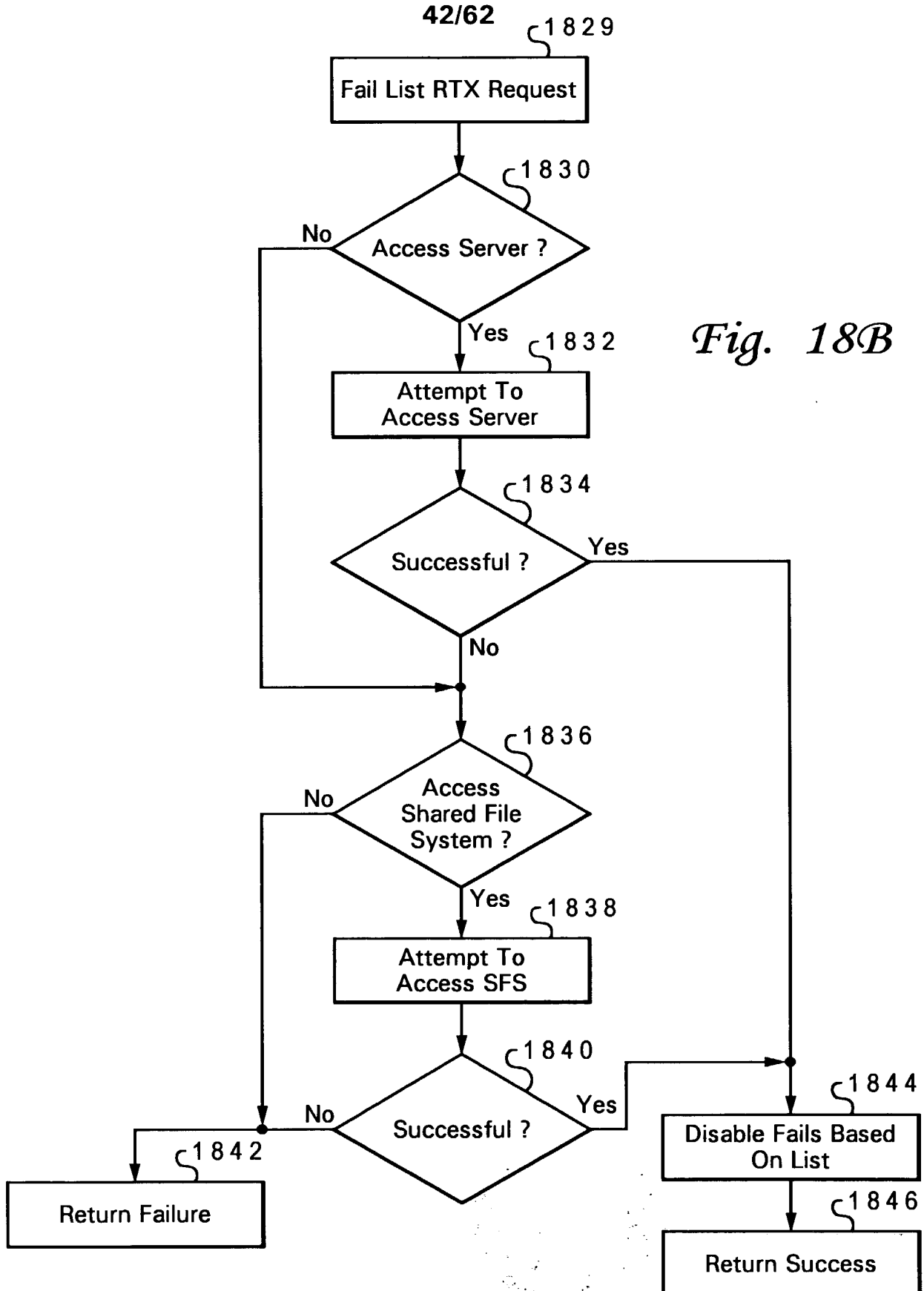


Fig. 18A

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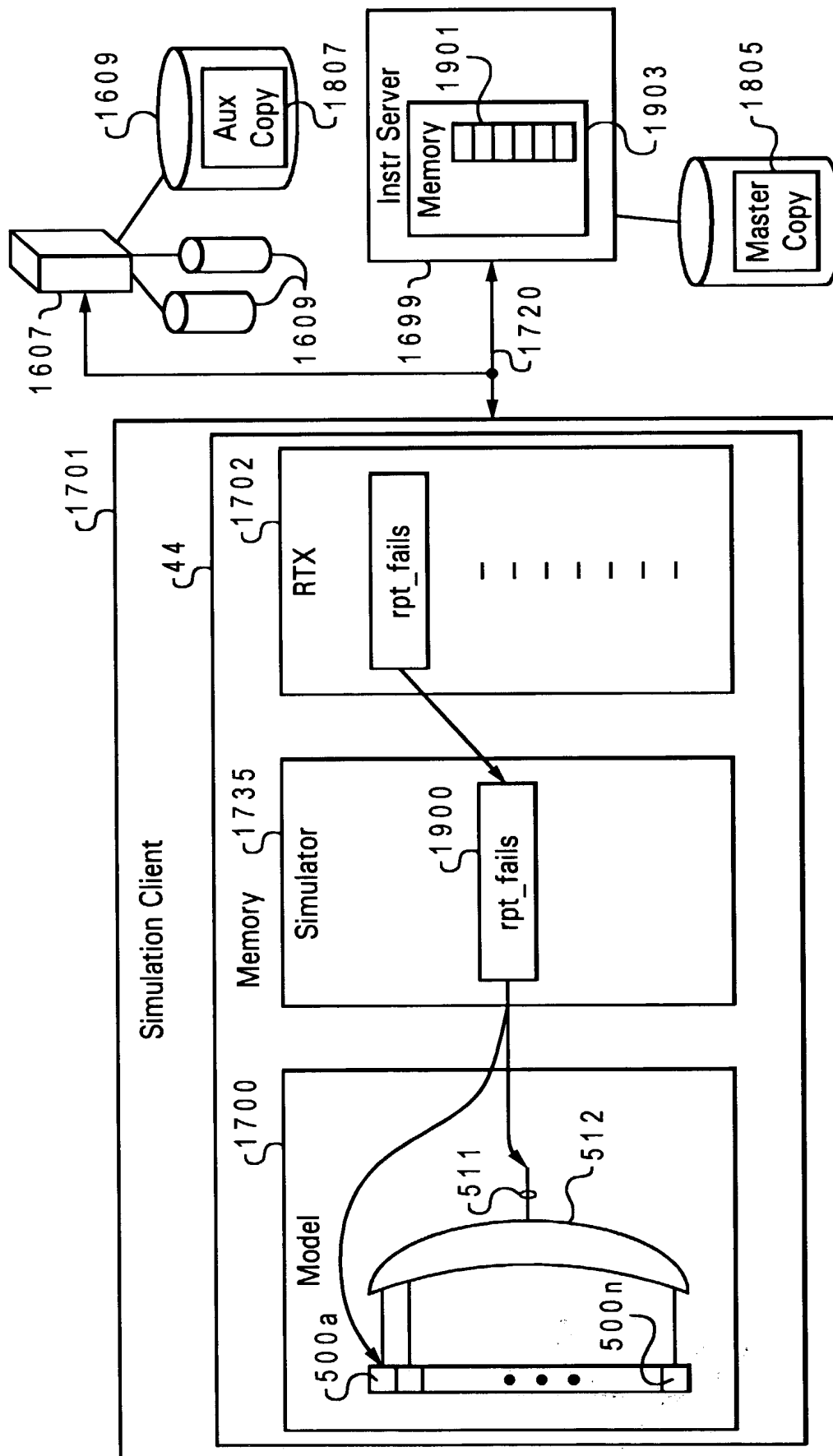
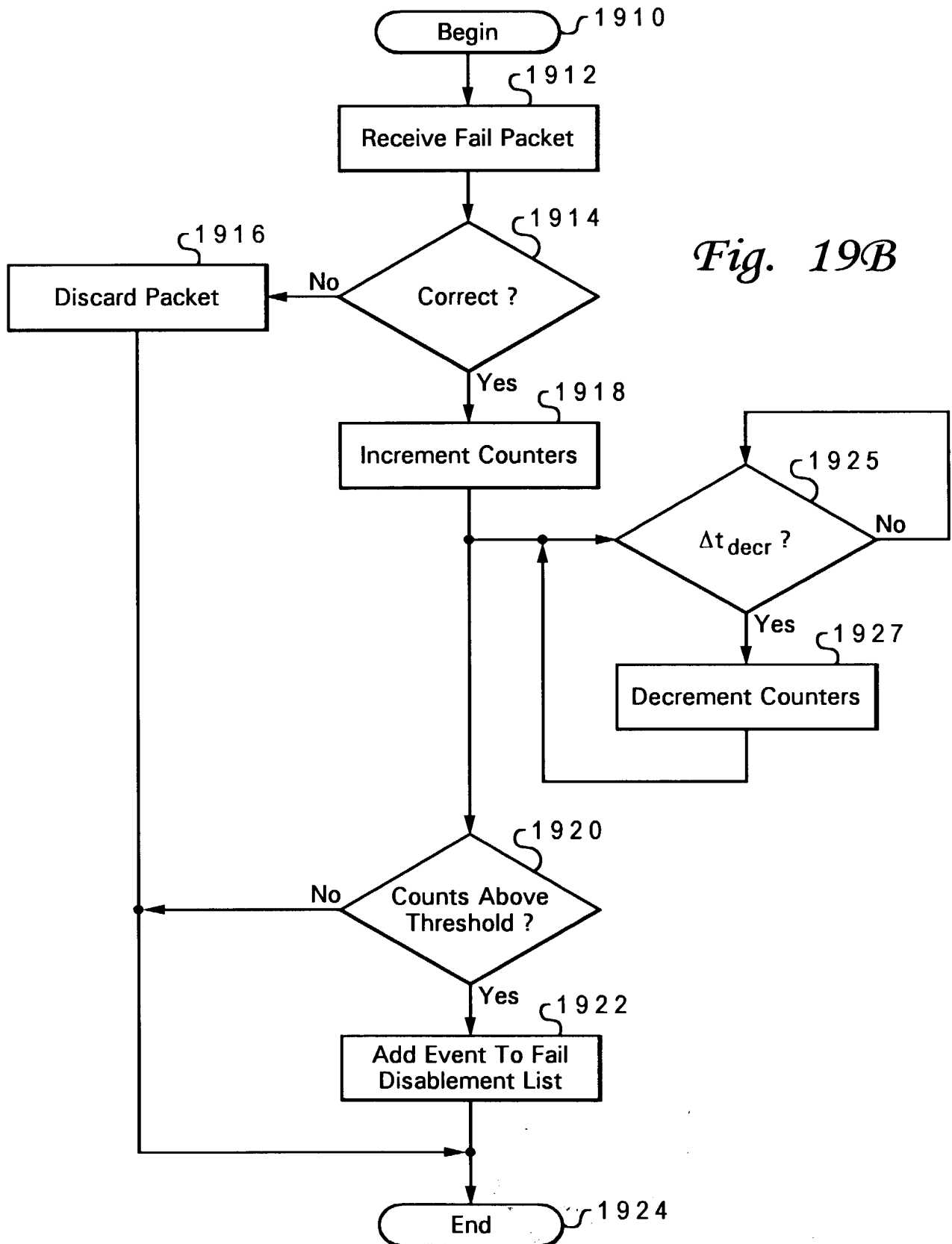


Fig. 19A

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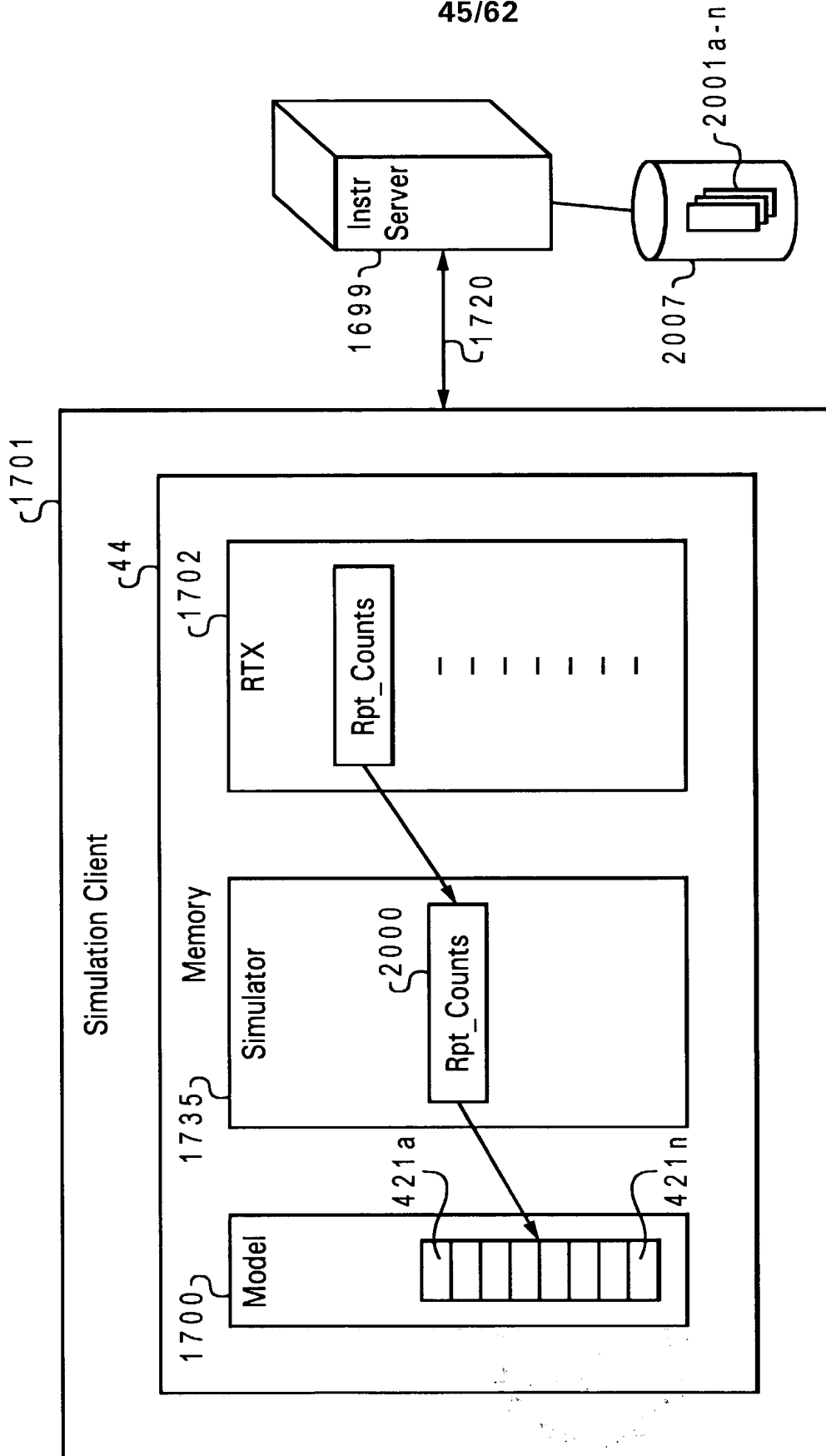


Fig. 20A

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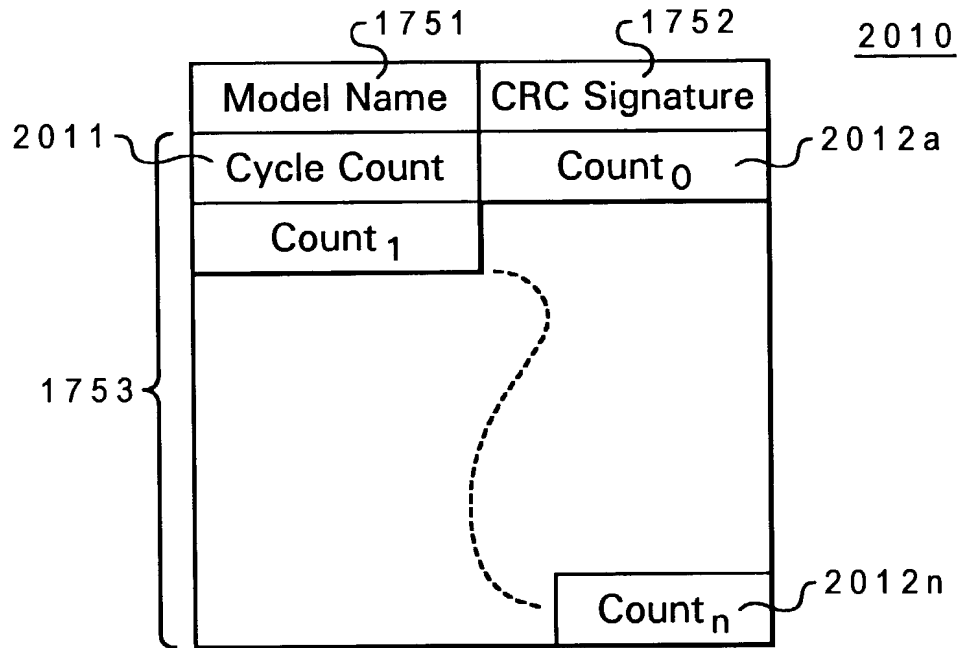


Fig. 20B

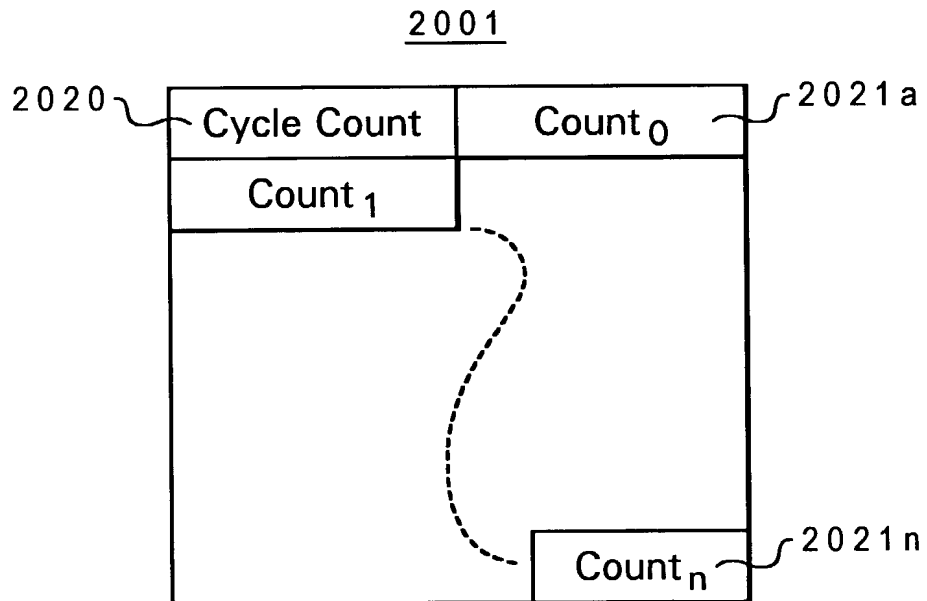


Fig. 20C

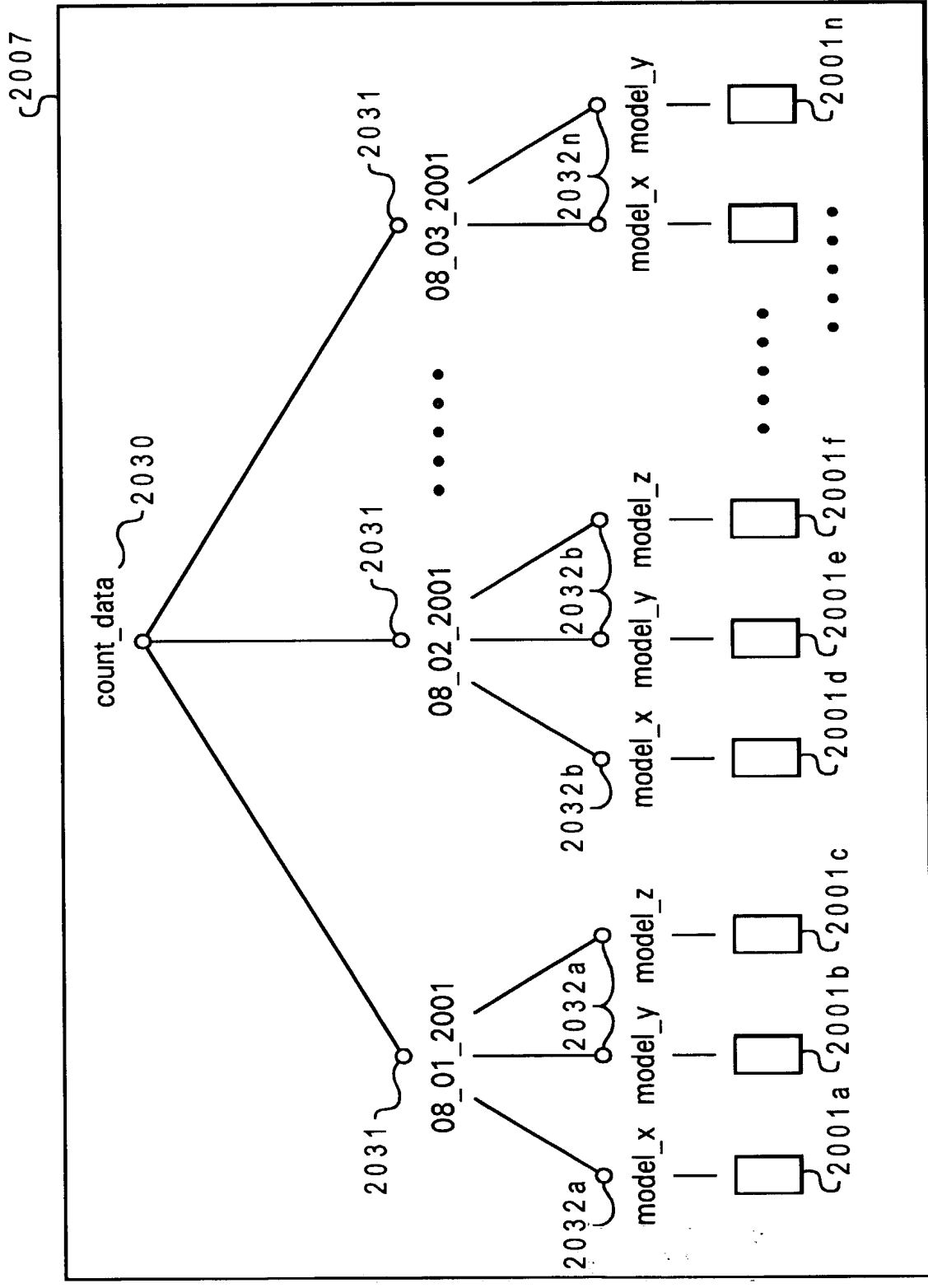


Fig. 20D

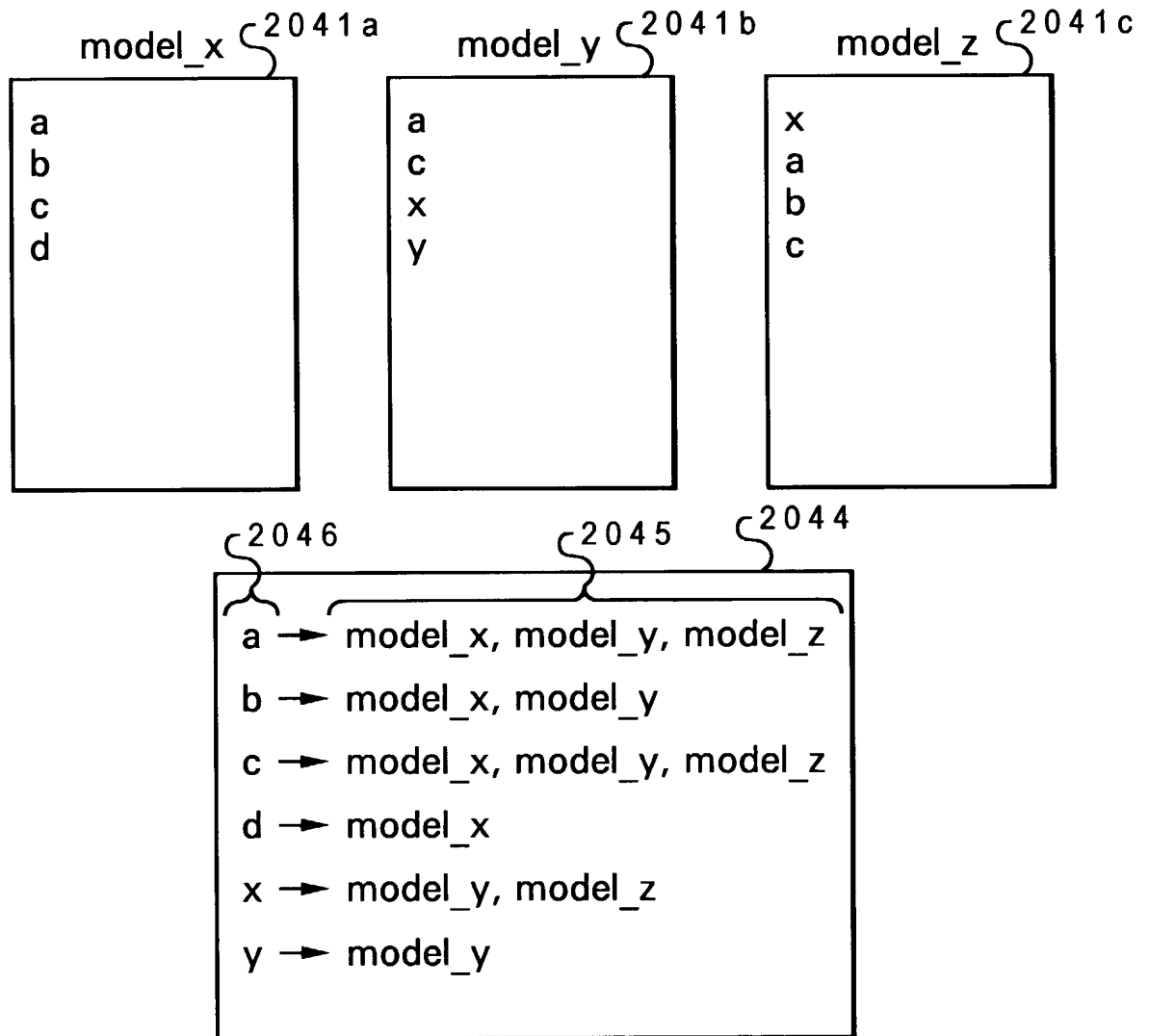
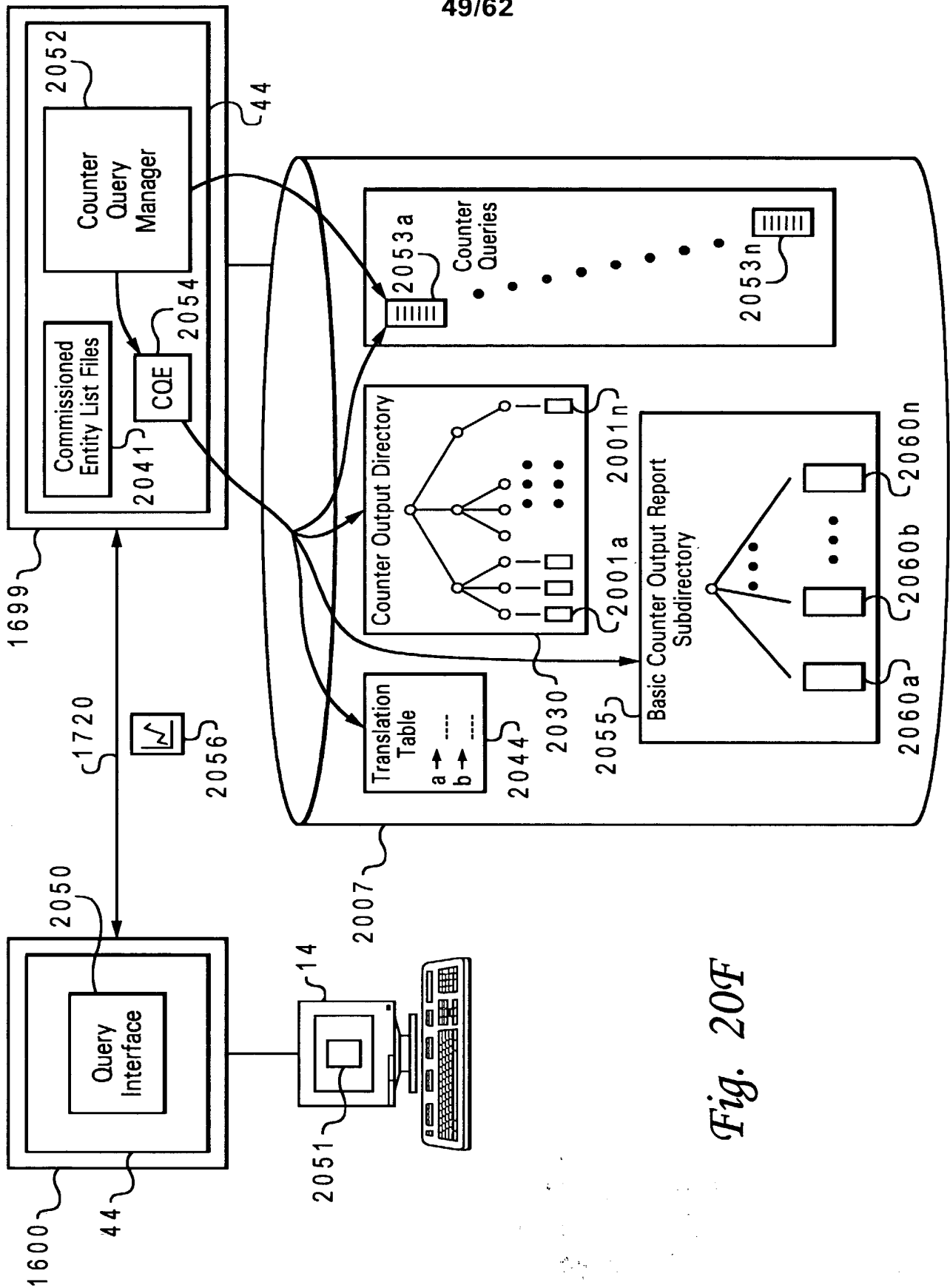
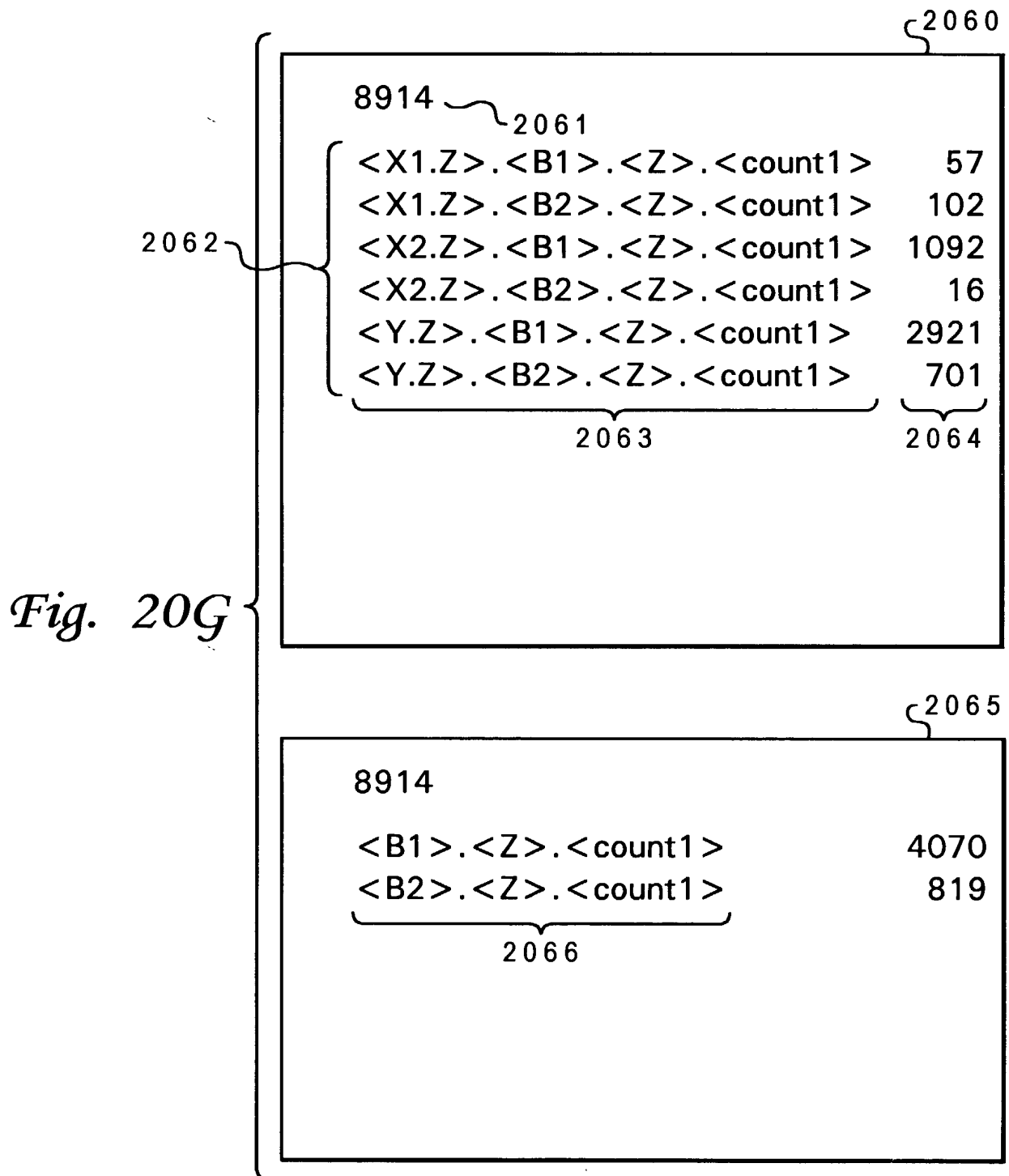


Fig. 20E





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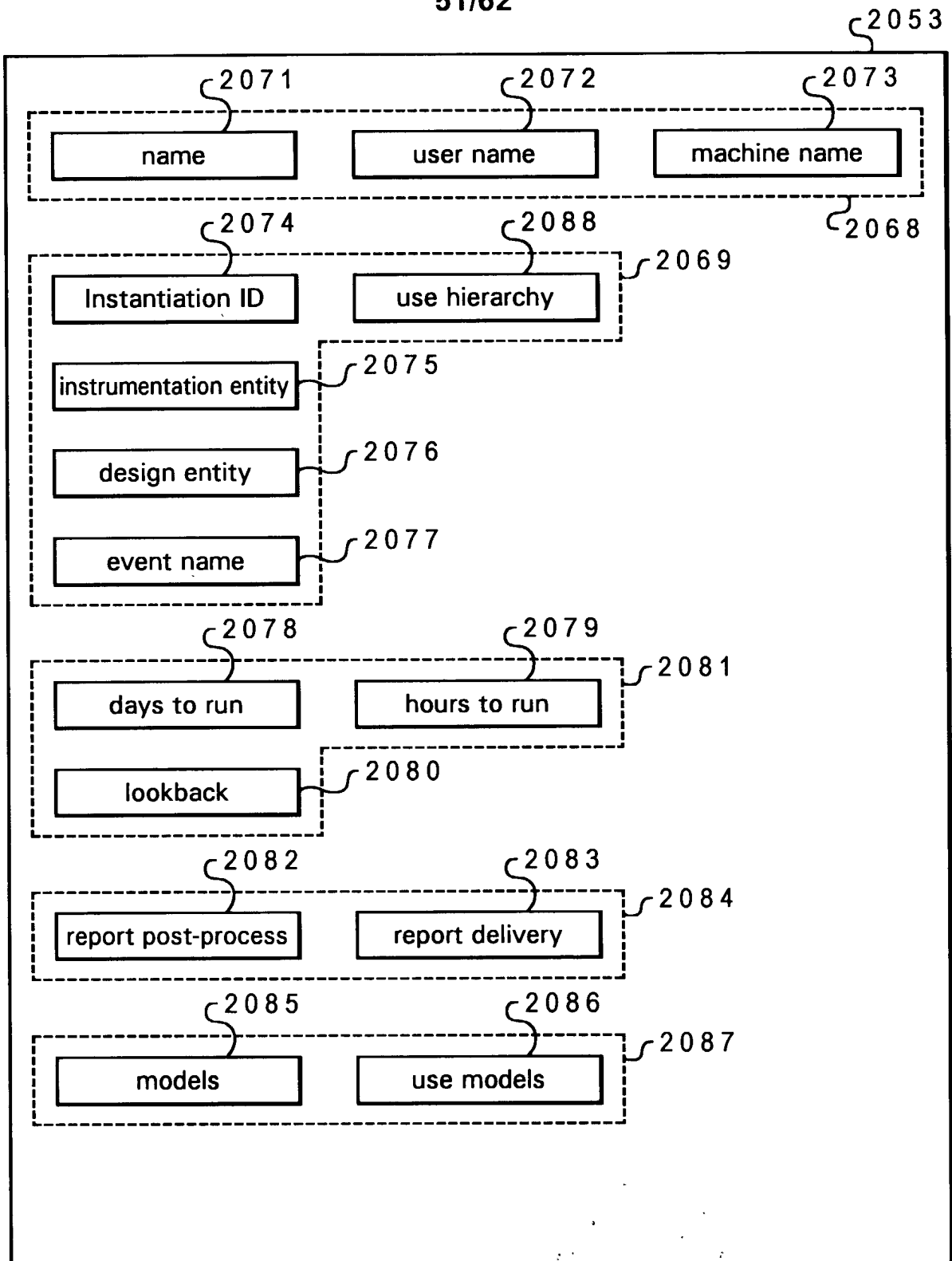


Fig. 20H

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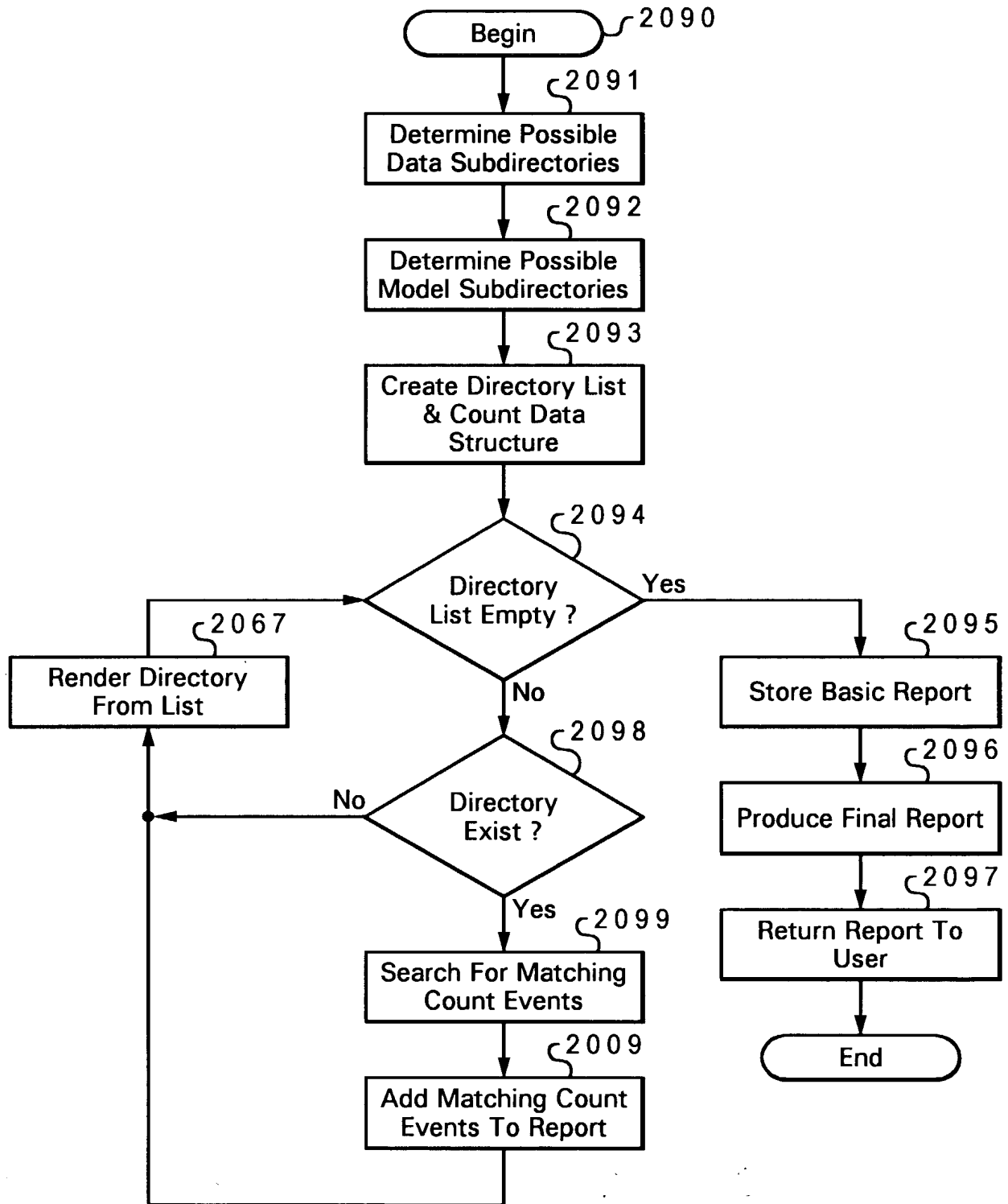
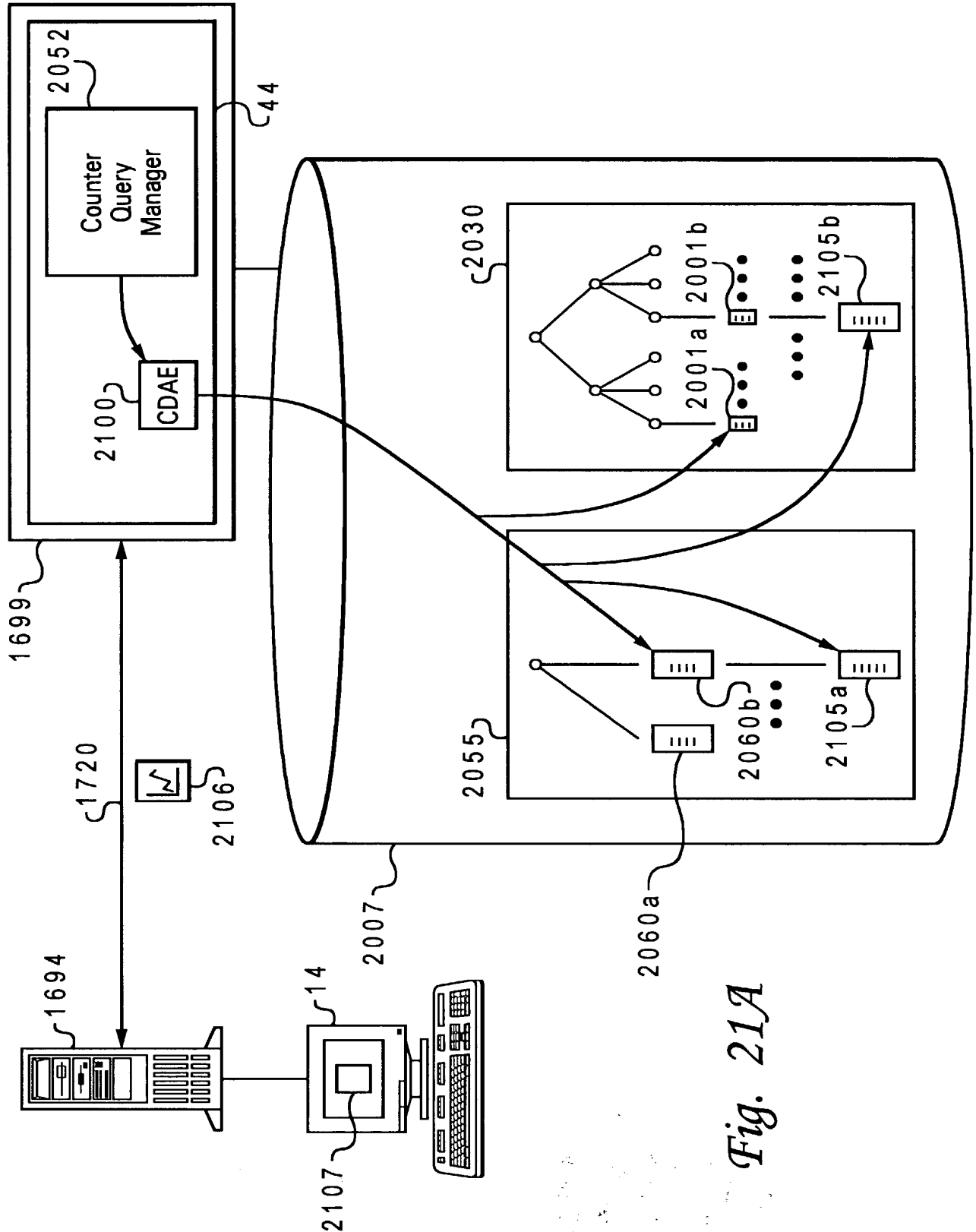


Fig. 20I



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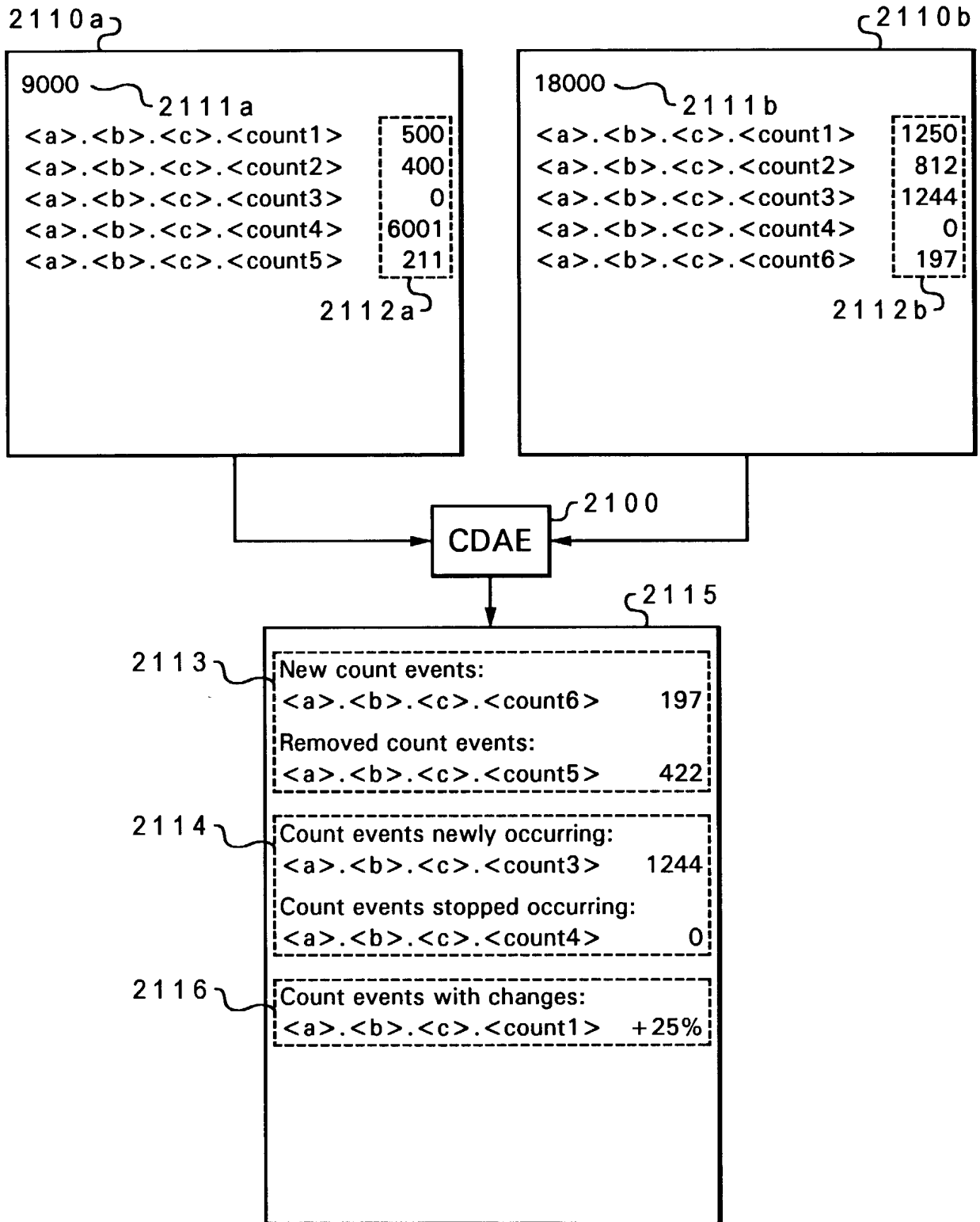


Fig. 21B

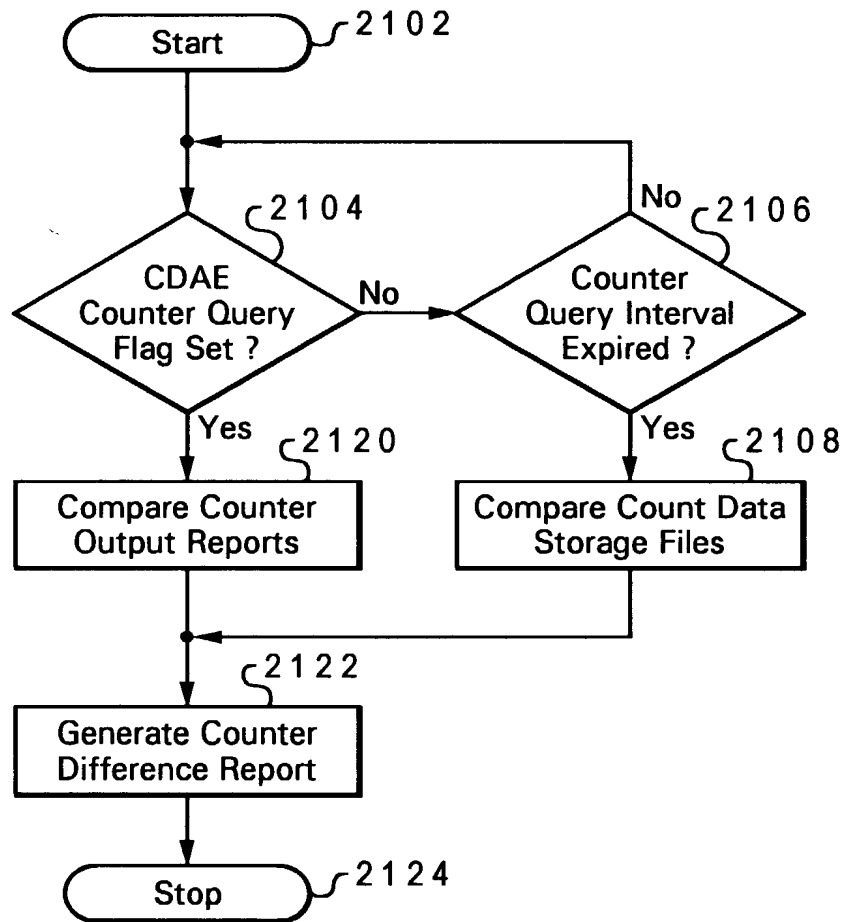
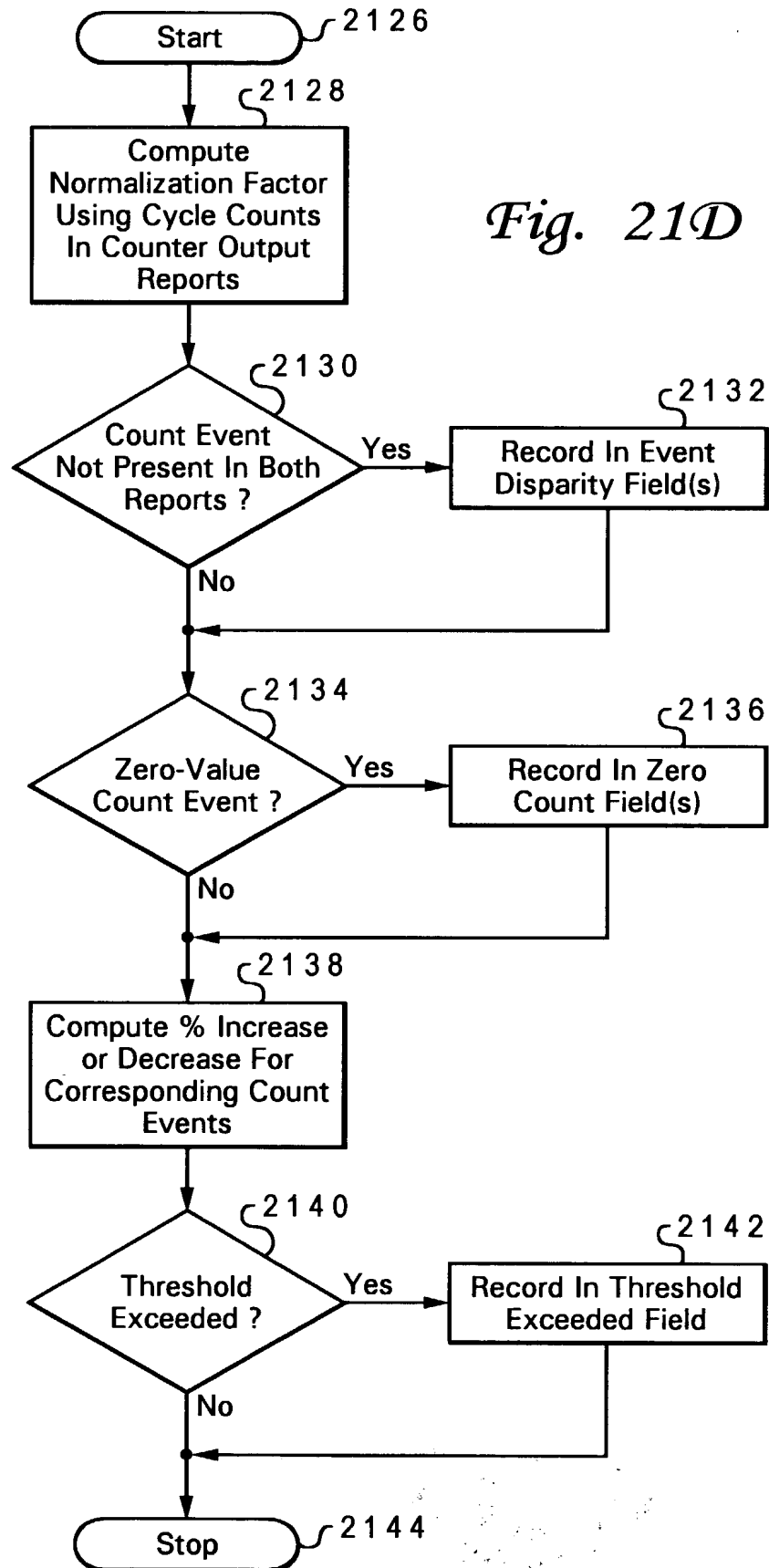


Fig. 21C



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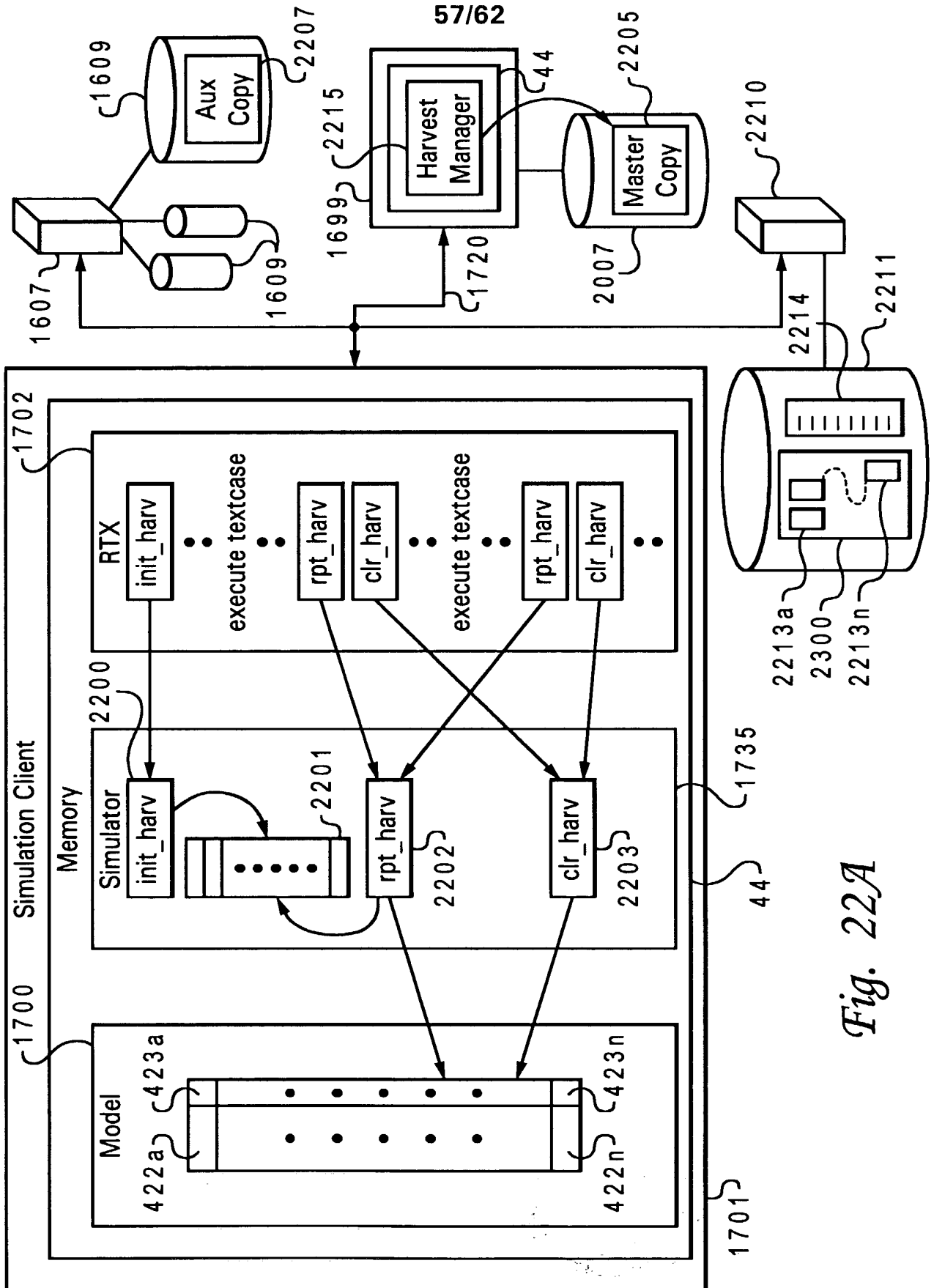


Fig. 22A

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2250

Begin

Fig. 22B

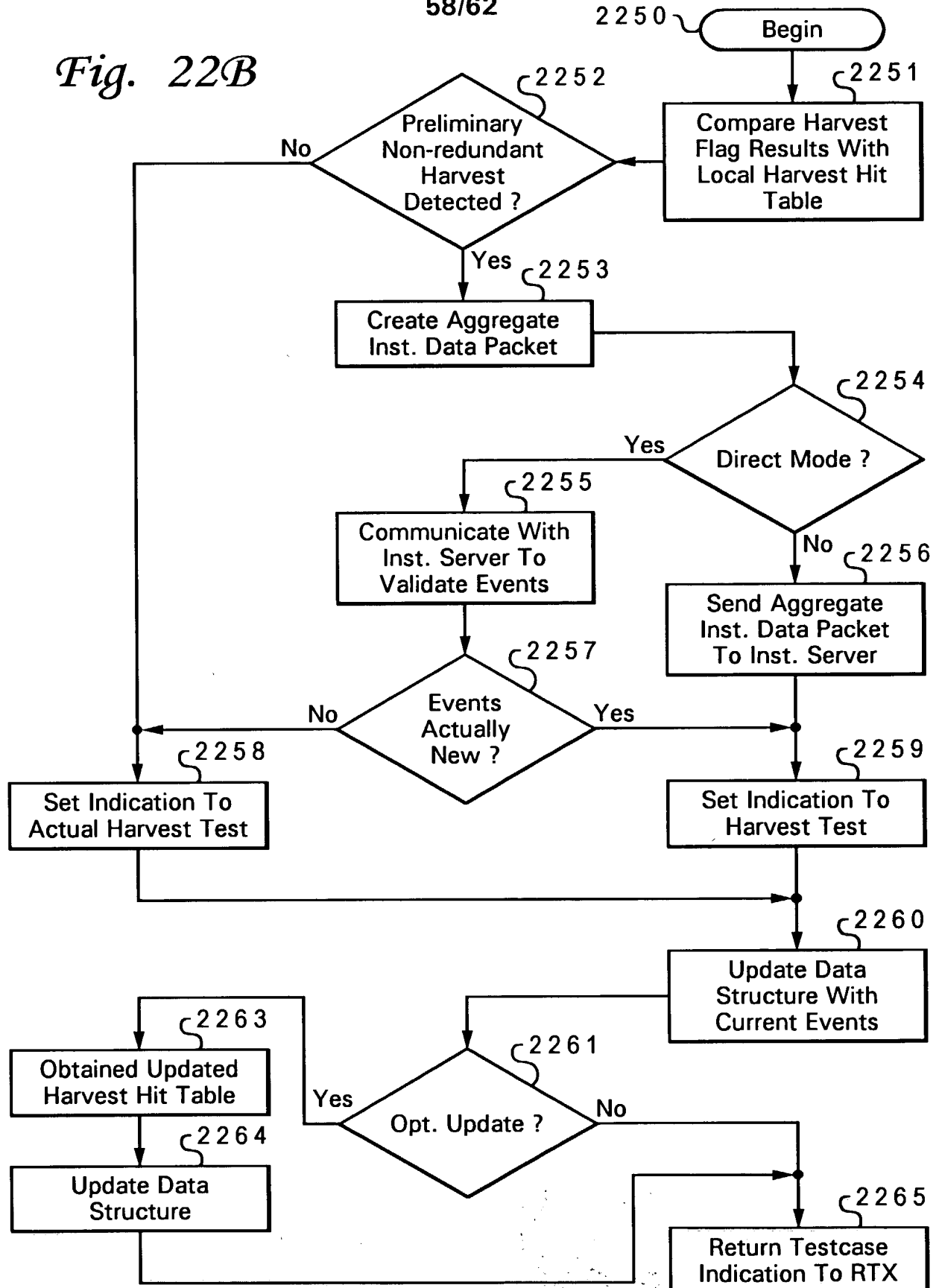
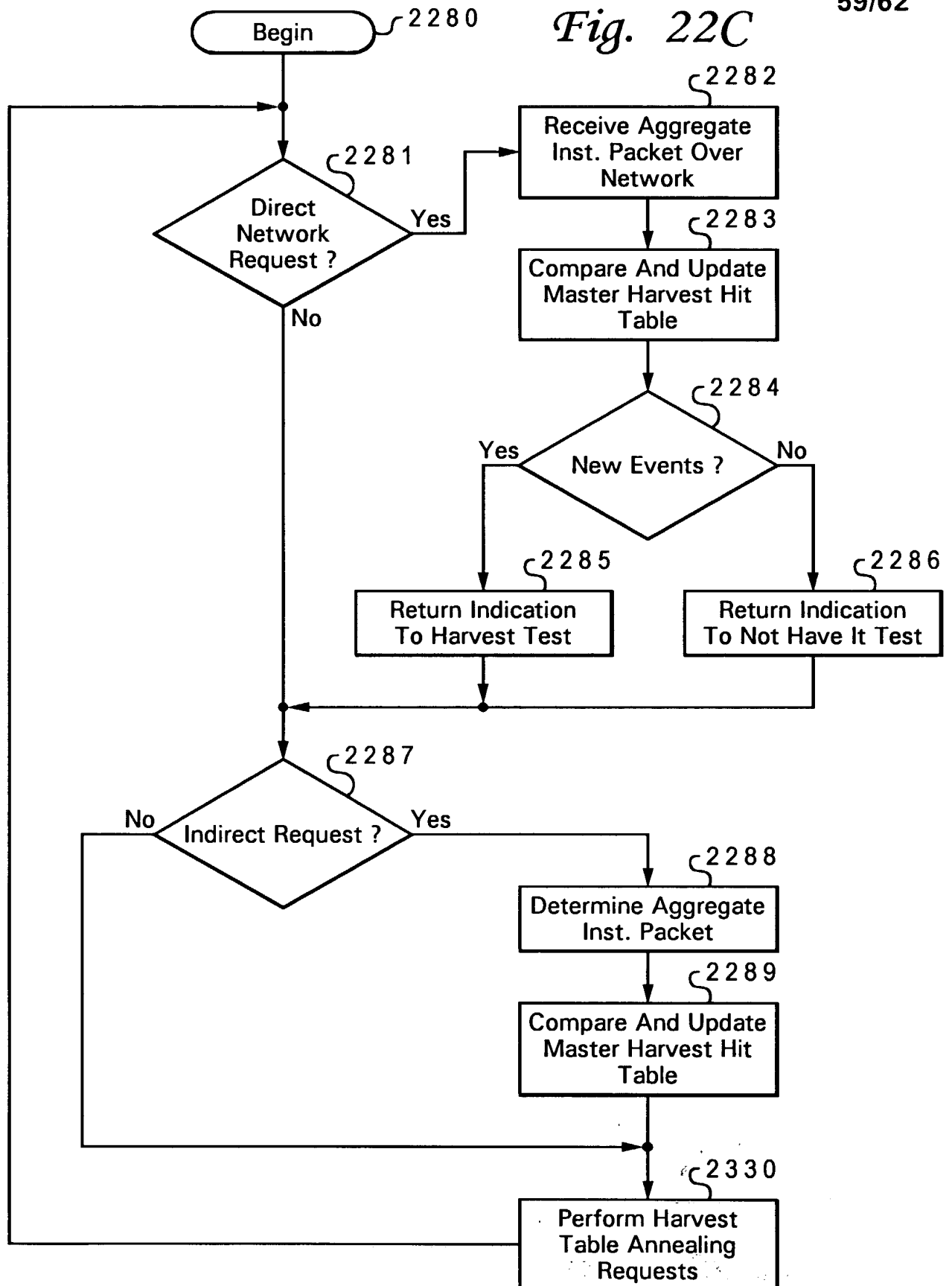


Fig. 22C



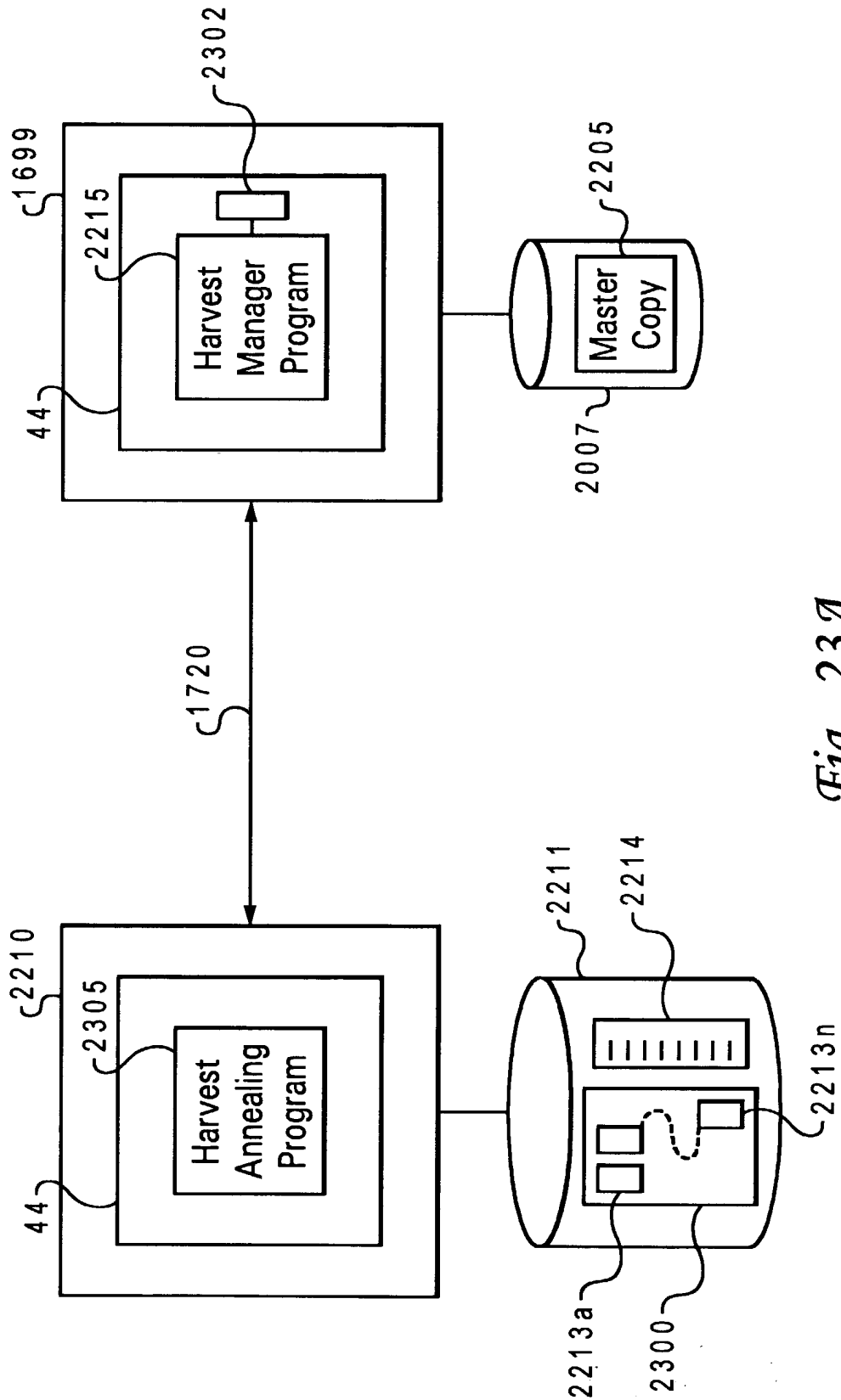


Fig. 23A

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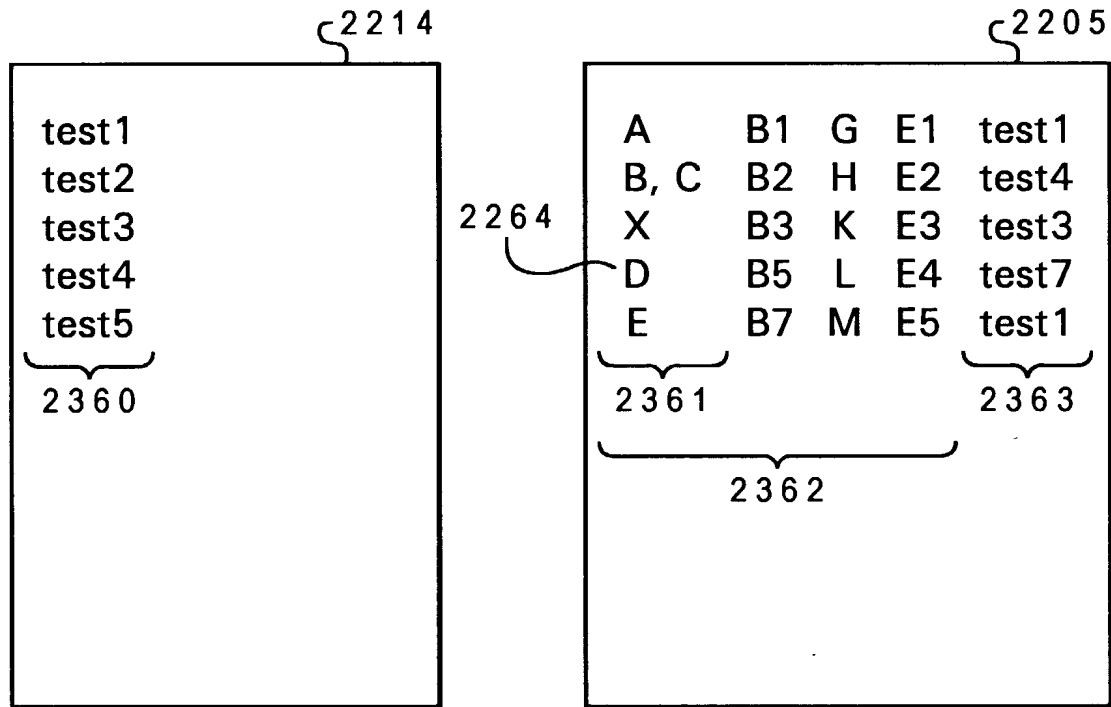


Fig. 23B

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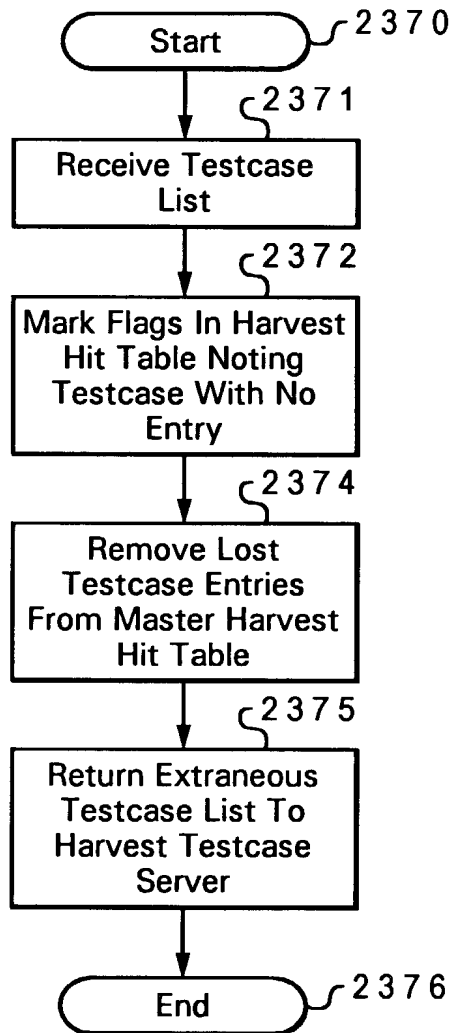


Fig. 23C